ANALOG DEVICES

RMS to DC Conversion Application Guide

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RMS TO DC CONVERSION APPLICATION GUIDE

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INTRODUCTION

This Application Guide sets forth the principles of operation and several representative applications of the AD536A, AD636, and AD637 integrated circuit true rms to dc converters. The low cost, low power consumption and high (laser trimmed) accuracy of these integrated circuits make rms computation a practical and accessible technique for extracting a measure of the power or the standard deviation of a waveform. Previously, the high cost and relative complexity of using modular, hybrid, or discrete component rms converters had tended to make "true rms" something of a laboratory curiosity restricted to specialized instruments.

In addition to specific applications, this guide also briefly covers the mathematics of rms and offers a comparison between various implementations of the rms equation, e.g., thermal, implicit and explicit computation, and the more commonly used "average" rectified value *non* rms detector. We hope that this background information will help remove some of the mystique of rms computation and assist the designer in applying the various Analog Devices rms converters and rms measurement in general in a creative and knowledgeable manner.

We gratefully acknowledge the support and assistance of the following people: Ernest Lehtonen and the Staff of the Analog Devices Graphic Services Art Department for the creative and clear rendering of the illustrations used in this guide, Julie Williams for typing and proofreading the manuscript, Paul Brokaw and Doug Grant for their careful review of the text, Don Travers and the ADS Applications Group for their many practical suggestions, and finally, Rich Frantz and George Adams for their support and encouragement during this lengthy project.

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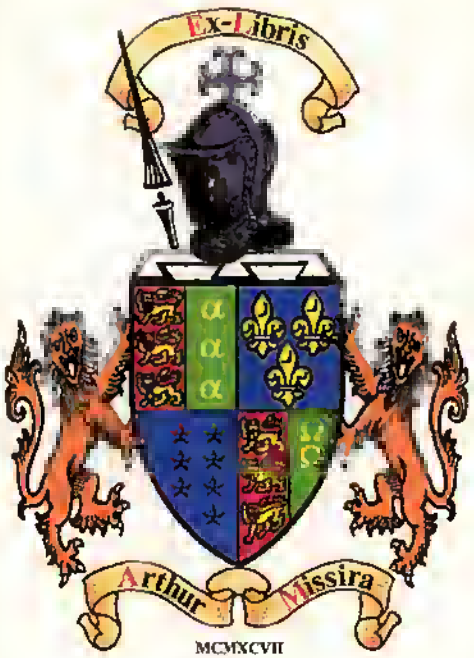

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SECTION I

RMS-DC CONVERSION – THEORY

BASIC DEFINITIONS

Definition of rms

RMS or Root Mean Square is a fundamental measurement of the Magnitude of an ac signal. Its definition can be both practical and mathematical. Defined Practically: the rms value assigned to an ac signal is the amount of dc required to produce an equivalent amount of heat in the same load. For example: an ac signal of 1 volt rms will produce the same amount of heat in a resistor as a 1 volt dc signal. Defined Mathematically: the rms value of a voltage is defined as:

$$E_{rms} = \sqrt{AVG.(V^2)}$$

(The above is a simplified formula–equivalent to the standard deviation of a zero average statistical signal.) This involves squaring the signal, taking the average, and obtaining the square root. The averaging time must be sufficiently long to allow filtering at the lowest frequencies of operation desired.

Definition of Crest Factor

The crest factor of a waveform is a ratio of its peak value to its rms value. Signals such as amplitude symmetrical squarewaves or dc levels have a crest factor of one. Other waveforms, more complex in nature, have higher crest factors, (see Table I).

RECTIFIER OR MAD (MEAN ABSOLUTE DEVIATION) METHOD OF AC MEASUREMENT (SEE FIGURE 1)

The most common method of measuring the magnitude of an ac signal is the precision rectifier approach which is actually a measure of the mean absolute deviation (MAD) or "ac AVERAGE" of a waveform. The gain or scale factor of the system is usually calibrated to the ratio of rms to MAD for sinewaves.

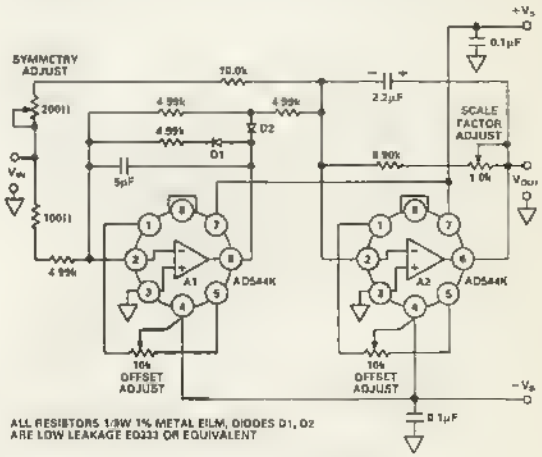


Figure 1. A Precision (MAD) Rectifier

Waveform 1 Volt Peak	RMS	MAD	RMS:MAD	Crest Factor
Undistored Sinewave	$\frac{V_{PEAK}}{\sqrt{2}} = 0.707$ Volts	$\frac{2V_{PEAK}}{\pi} = 0.636$ Volts	$\frac{0.707}{0.636} = 1.11$	$\frac{V_{PEAK}}{V_{rms}} = 1.414$
Symetrical Squarewave	$\frac{V_{PEAK}}{1} = 1.00$ Volts	$\frac{V_{PEAK}}{1} = 1.00$ Volts	$\frac{1.00}{1.00} = 1.00$	$\frac{V_{PEAK}}{V_{rms}} = 1.00$
Undistored Triangle-Wave	$\frac{V_{PEAK}}{\sqrt{3}} = 0.580$ Volts	$\frac{V_{PEAK}}{2} = 0.500$ Volts	$\frac{0.580}{0.500} = 1.155$	$\frac{V_{PEAK}}{V_{rms}} = 1.73$

Table I. RMS, MAD and Crest Factor Chart

This works fine as long as the input waveform is an undistored sinewave; for any other waveform, the ratio of rms/MAD changes, and serious errors develop.

For these reasons, the precision rectifier method provides only a relative measure of the amplitude of non-sinusoidal waveforms.

For a graphic comparison of the performance of an MAD rectifier vs. a true rms converter over varying duty cycles see Figure 10 in Section II of this guide.

METHODS OF TRUE RMS-DC CONVERSION

Thermal rms-dc Conversion

Thermal conversion is the simplest method in theory; yet, in practice, it is the most difficult and expensive to implement. This method involves comparing the heating value of an *unknown* ac signal to the heating value of a *known* calibrated dc reference voltage. When the calibrated voltage reference is adjusted to null the temperature difference between the reference resistor (R_2) and the signal resistor (R_1), the power dissipated in these two matched resistors will be equal. Therefore, by the basic definition of rms, the value of the dc reference voltage will equal the rms value of the unknown signal voltage.

Each thermal unit contains a stable, low-TC resistor (R_1, R_2) which is in thermal contact with a linear temperature to voltage converter, S_1, S_2. (For example, a thermocouple.) The output voltage of S_1 (S_2) varies in proportion to the mean square of V_{IN}. (The first order temperature/voltage ratio will vary as K V_{IN}/R_1.)

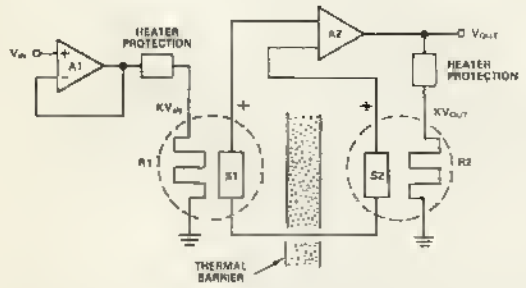


Figure 2. A Thermal rms to dc Converter

The circuit of Figure 2 typically has very low error (approximately 0.1%) as well as wide bandwidth. However, the fixed time constant of the thermal unit (R_1 S_1, R_2 S_2) limits the low frequency effectiveness of this rms computational scheme.

In addition to the basic types discussed, there are also variable gain thermal converters available which can overcome the dynamic range limitations of fixed gain converters at the expense of increased complexity and cost.

Various Computing Methods of rms-dc Converters

Direct or Explicit Computation

The most obvious method of computing rms value is to perform the functions of squaring, averaging, and square rooting in a straight-forward manner using multipliers and operational amplifiers. The direct or *explicit* method of computation (Figure 3) has a limited dynamic range because the stages following the squarer must try to deal with a signal that varies enormously in amplitude. For example, an input signal that varies over a 100 to 1 dynamic range (10mV to 1V) would have a dynamic range of 10,000 to 1 at the output of the squarer (squarer output = 1mV to 10 volts). These practical limitations restrict this method to inputs which have a maximum of approximately 10;1 dynamic range. System error can be as little as ±0.1% of full scale using a high quality multiplier and square rooter. Excellent bandwidth and high speed accuracy can also be achieved using this method.

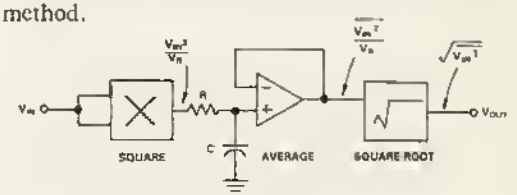


Figure 3. The Explicit Computation Method

Indirect or Implicit Computation

A generally better computing scheme uses feedback to perform the square root function implicitly or indirectly at the input of the circuit as shown in Figure 4. Divided by the average of the output, the *average* signal levels now vary *linearly* (instead of as the *square*) with the rms level of the input. This considerably increases the dynamic range of the implicit circuit, as compared to explicit rms circuits.

Some advantages of implicit rms computation over other methods are fewer components, greater dynamic range, and generally lower cost. A disadvantage of this method is that it generally has less bandwidth than either thermal or explicit computation. An implicit computing scheme may use direct multiplication and division (by multipliers), or it may use any of several log-antilog circuit techniques.

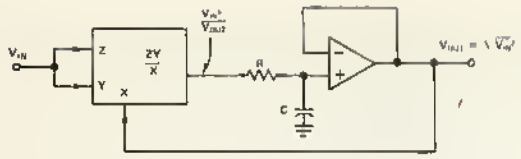


Figure 4. The Implicit Computation Method

MONOLITHIC RMS TO DC CONVERTERS – PRINCIPLES OF OPERATION

AD536A – Wide Range rms Converter

The AD536A uses an implicit method of rms computation employing an absolute value V/I converter, a squarer divider, low pass filter, precision current mirror, and an output buffer (see Figures 5 and 32). It features a 10 volt full scale input range.

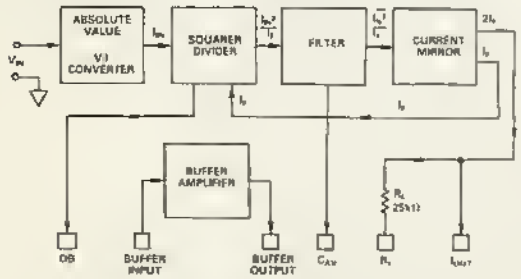


Figure 5. AD536A/AD636 Block Diagram

The voltage input to the AD536A is first processed by an absolute value circuit (a precision rectifier) which has a single polarity output. This output drives a voltage to current converter (an operational amplifier) whose current output, I_{IN}, is the rectified input signal.

Current I_{IN} drives a squarer/divider, which performs both the squaring and square rooting functions in one stage by utilizing feedback from the current mirror. The feedback current, I_F, is divided into the squared input current, I_{IN}^2, using log-antilog circuits. Since dB or decibels are a function of the log of a signal, a dB output for the AD536A is derived from this squarer/divider stage. The output from this stage, I_{IN}^2/I_F, is averaged by a low pass filter consisting of an internal resistor and an externally-connected filter capacitor. This filtered signal drives the current mirror which provides the feedback current, I_F, and the output current, $2I_F$. The output current is set at twice the feedback current to develop the desired output voltage for the device using its internal 25kΩ resistor, R_L. The I_{OUT} pin of the AD536A gives a current output of 400μA per volt of rms input signal. Grounding the R_L pin gives a voltage output of 1 volt dc per volt rms input. The unity gain buffer amplifier may be used to provide a low impedance voltage output for either the I_{OUT} or dB output function.

AD636 – Low Power/Low Level Operation rms Converter

The AD636 low-power rms converter is very similar to the standard AD536A, however, it is optimized for low level, low power operation in portable instruments; it features a 200mV full scale input range.

AD637 – High Performance rms Converter

The AD637 has higher accuracy (than the AD536A), an extended frequency response, and a −3dB bandwidth as high as 8MHz (see Table 2). This converter (Figure 6) uses an inverting low pass filter stage to provide a buffered voltage output whose averaging time constant is independent of input signal level (unlike the AD536A and AD636).

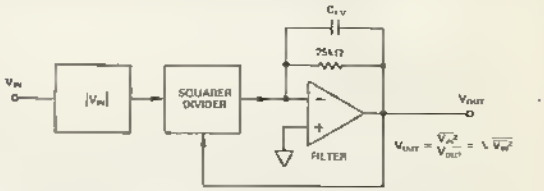


Figure 6. AD637 Filter/Averaging Diagram

In addition to improved overall performance, the AD637 contains two unique features: a denominator input provision which allows this rms converter to operate as a squarer, mean squarer, root sum of squares (vector sum) and also facilitates low frequency (10Hz) measurement. A second feature, an optional chip select provision, allows the user to power-down the rms converter to conserve power when it is not being used (as in portable meters on dc ranges). The chip select is normally *on* and must be pulled *low* to a TTL input level of 0.8 volts or less to put the rms converter in the stand-by state reducing its power consumption by 7 to 1. For normal operation without the chip select provision, this pin should be left floating. The output (pin 9) goes to a high impedance state when the chip select is low. This analog "three state" operation permits the outputs of several AD637s to be connected in parallel and allows the desired channel to be selected by pulling its chip select high, thus creating an active multiplexer. Like its predecessors, the AD637 full wave rectifies the input signal voltage using an absolute

value circuit. As shown in Figure 7, the next section of the converter takes the log of this dc signal and doubles it, performing a squaring operation. The squared output of this section then passes on to a divider stage where the log of the rms output V_{OUT} is subtracted from the log of the squared input signal. An exponential section then takes the antilog leaving: V_{IN}^2/V_{OUT}.

This is applied to the final section of the rms converter, a filter stage which takes the average of this processed signal leaving: $\overline{V_{IN}^2}/V_{OUT}$.

And since at the output:

$$V_{OUT} = \frac{\overline{V_{IN}^2}}{V_{OUT}}$$

then:

$$V_{OUT} = \sqrt{\overline{V_{IN}^2}}$$

(V_{OUT} times both sides of the equation)

This is, by definition, the rms value of the input voltage.

Some additional comments:

The denominator input is normally connected to the V_{OUT} pin, as shown by the dotted lines in Figure 7, to perform the V_{IN}^2/V_{OUT} function. However, if the denominator input, which controls the scale factor, is connected to a fixed dc voltage, V_{EXT}, the output will be: $\overline{V_{IN}^2}/V_{EXT}$. This is equal to the mean square of the input divided (or multiplied if $-V_{EXT}$ is used) by a fixed scale factor.

The filter stage of the AD637 consists of an operational amplifier/integrator whose averaging time constant is set by its internal on-chip 25kΩ feedback resistor and an external averaging capacitor, C_{AV}. The RC_{AV} time constant should be chosen to be longer than the period of the lowest frequency being measured, yet short enough to allow tolerable settling time. Since the filter stage output impedance is low, further output buffering is not necessary. The on-chip buffer amplifier is normally needed only in applications where an active filter is required to further reduce the output ripple (see Filters and Averaging section.)

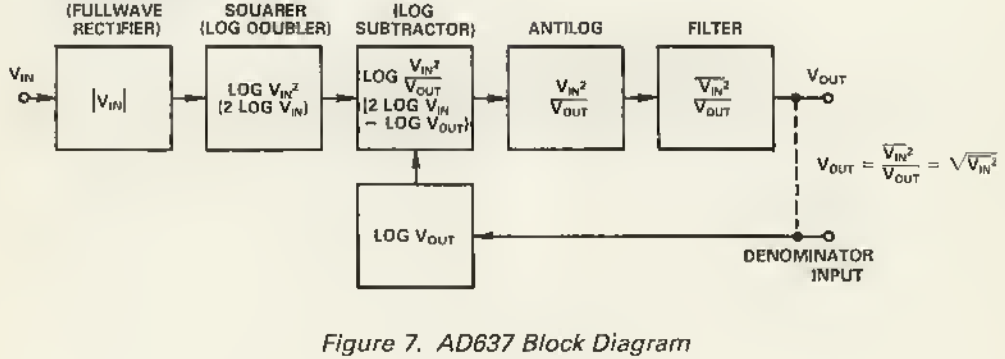


Figure 7. AD637 Block Diagram

SECTION II

RMS-DC CONVERISON – BASIC DESIGN CONSIDERATIONS

ACCURACY OF RMS-DC CONVERTERS

An ideal rms converter would provide a "dc" output voltage exactly equal to the rms value of its input voltage, regardless of the amplitude, frequency, or wave shape of the input waveform. Of course a practical rms converter does have some errors. In the following sections, we will discuss these errors and their overall effect on rms converter performance.

First, we will discuss the low frequency or "static" errors. Next, we will review the affects of bandwidth on accuracy. Then, we will present in some detail the affect of the converter's averaging time constant. Finally, we will discuss the affect of wave shape, e.g., pulses, noise, SCR controlled sinewaves, on the rms converter's accuracy.

"Static" Errors – rms-dc Converter Static Errors and Their Effect on Overall "Accuracy"

Static errors are those offsets and scale factor errors which apply to "dc" or moderate frequency (≃1kHz) sinewave input signals. Under these conditions, the finite bandwidth of the converter (and the effective averaging time) can be made negligible compared to the input, output, offset, and scale factor errors. RMS can be interpreted here as the square root of the low pass filtered (or averaged) square of the input signal voltage.

An rms to dc converter's overall "static" error is specified in percent of reading plus a constant. As shown by Table 2, the AD637J is specified at 1.0mV ±0.5% of reading. This should be interpreted to mean that *at any* point within the AD637J's 0V to 7V rms input dynamic range, the converter's output voltage will differ (at most) from the precise value of the rms input by 1mV *plus* 0.5% of the *correct rms level*. Note that this is less absolute error than the AD536AJ rms converter. To illustrate this point, consider a sinewave input of 1.00V rms at 1kHz applied to the input of an AD637J. The actual AD637 output voltage will be within: ±(1.0mV + 0.5% × 1.0V) = ±(1mV + 5mV). This equals 6mV from the ideal output of 1.0V or between 0.994 volts and 1.006 volts dc. This error performance is summarized in the graph of Figure 8 which shows error versus input level in the AD637K and AD536J rms-dc converters.

	AD536AJ	AD637J	AD636J
Nominal Full Scale Peak Trans. Input Max Total Error No External Trim	2V rms ±20V 5mV ±0.5% RDG	2V rms ±15V 1mV ±0.5% RDG	200mV rms ±2.8V 0.5mV ±1% RDG
Bandwidth, (–3dB) Full Scale 0.1V rms	 2MHz 300kHz	 8MHz 600kHz	 1.3MHz 800kHz
Error at Crest Factor of 5	–0.3% @ 1V rms	±0.15% @ 1V rms	–0.5% @ 200mV rms
Power Supply Volts Current	 ±3 to ±18 max 1mA; 2mA max	 ±3 to ±18 max 2mA; 3mA max	 +2, –2.5, ±12 max 800μA; 1mA max

Table 2. Condensed rms Converter Specifications Table

These static errors can be classified into the standard categories of offset, voltage, scale factor (gain) error, and nonlinearity errors.

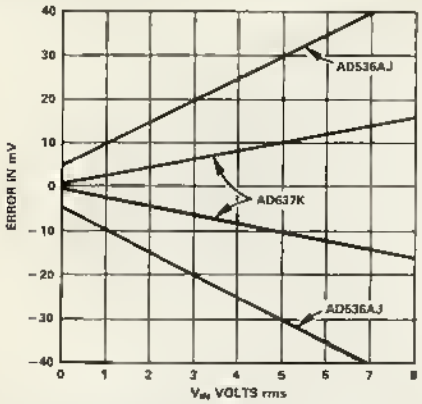


Figure 8. Maximum Error vs. Input Level AD637K and AD536AJ rms Converters

Every *practical* rms converter will have an input/output transfer characteristic that deviates from the ideal. The detailed error explanation given by Figures 9a and 9b illustrate the major classes of errors which are commonly encountered. At low levels, the rms converter's input offset voltages can flatten the point of the ideal absolute value transfer and shift it up (or more positive) from the zero output voltage level with zero input voltage applied (see Appendix A). The practical effects of these offset errors determine both the resolution and accuracy of the converter for low level input signals.

For the ICs discussed in this guide, the combined total of offset errors is typically less than 1mV (refer to the data sheets for maximum specs). At higher input levels, those in the order of few hundred millivolts, scale factor and linearity errors may dominate offset errors. A scale factor error is defined as the difference between the average slope of the actual input/output transfer and the ideal 1 to 1 transfer, i.e., if a 100mV rms change in input voltage produces a 99mV change in output level, then the scale factor error is −1%.

In addition to the single polarity example just given, there can be a different scale factor for both negative and positive input voltages. The difference in these scale factors, termed the "dc reversal" error, is shown in Figure 9c. When testing this parameter, a dc voltage is applied to the converter's input, say +2V, and then the polarity of the input voltage is reversed (to −2V); the difference in the two readings will equal the dc reversal error. That is:

$$\text{dc reversal error} = \frac{(V_{OUT} + 2V\,\text{INPUT}) - (V_{OUT} - 2V\,\text{INPUT})}{2\,\text{VOLTS}} \times 100\%$$

The last remaining "static error" term is nonlinearity. As its name implies, it is the curved portion of the input/output transfer characteristic; this is shown in an exaggerated form in Figure 9c. This error is due to nonideal behavior in the rms computing section *and cannot be reduced by trimming offset or scale factor*. Therefore, nonlinearity sets a limit on the ultimate best-ease accuracy of the rms converter. The nonlinearity of the AD637 is typically 1mV (0.05%) over a 2V full scale rms range; for the

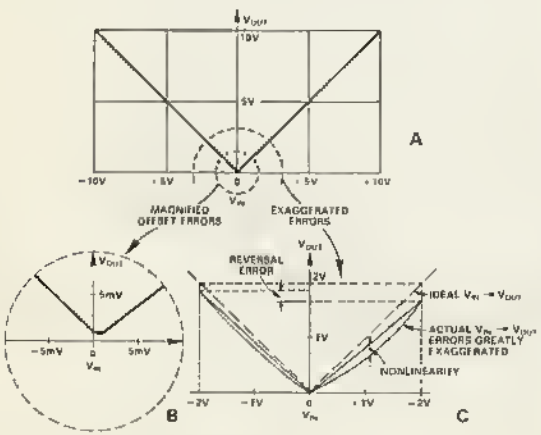


Figure 9. Static Errors in rms to dc Converters

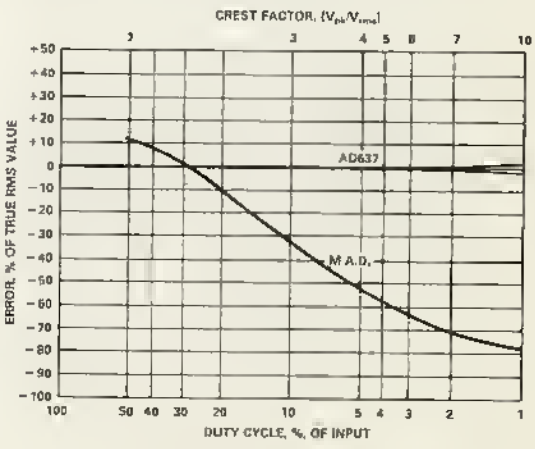


Figure 10. Error vs. Duty Cycle AD637 rms Converter and MAD ac Detector

AD536A the nonlinearity equals 5mV or less. The AD636 typically has less than 1mV nonlinearity over its 0 to 200mV specified input range.

As shown by Figure 10, the errors of true rms to dc converters, although varied, are considerably lower than those errors found in precision "MAD" rectifiers when the duty cycle of the input waveform is varied.

Bandwidth Considerations

So far, we have focused on errors for response to dc inputs, yet in practice ac inputs are of the most interest to users of rms converters.

For the case of 1kHz sinewave inputs, there is negligible difference between readings at this frequency

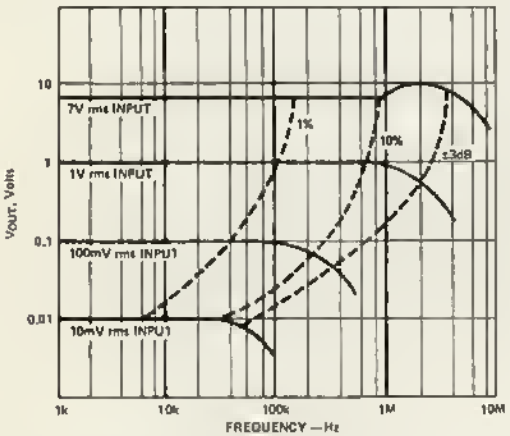


Figure 11. AD536A High Frequency Response

and performance with dc voltages applied, i.e., the 1kHz performance is very close to that of the static error performance with dc inputs so that dc measurements provide a convenient means of determining errors at ≈1kHz input frequencies. At higher input frequencies, however, the bandwidth characteristics of the rms converter become most important. As shown by Figures 11, 12, and 13, ac bandwidth drops off as the input level is reduced; this is primarily due to gain bandwidth limitations in the absolute value circuits. The AD637 and AD636 both achieve greater bandwidths on low level signals than the AD536A. The AD637 maintains this advantage at levels of one volt and above; while the AD636 is limited to 200mV full scale (its low level bandwidth is greater than the AD536A and it does have overrange operation to one volt with some degradation of accuracy.)

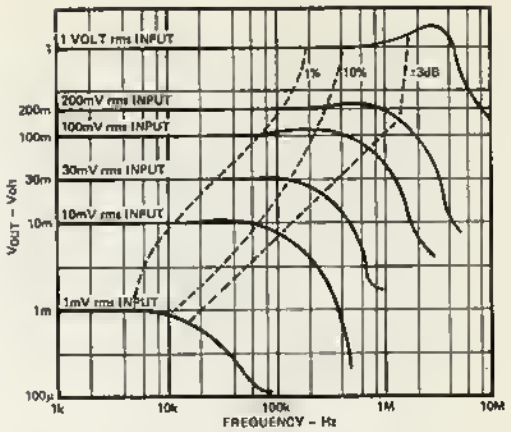


Figure 12. AD636 High Frequency Response

To achieve the maximum bandwidth for a particular application, the input signal of the system or instrument being used should be amplified (or attenuated) so that the maximum rms signal level corresponds to the rms converters full scale input level. The AD536A and The AD637 can be used at up to 7 volts full scale, however, a 2 volt full scale range allows for more headroom on peak inputs (high crest factor signals). These are usually limited by the clipping level of the input preamplifier to ± 12 volts. The AD536A and AD637 will not clip with up to ± 20 volt signals. Nevertheless, a 7 volt rms input signal with a crest factor of only 3 will have a 21 volt peak input level–overloading these devices! Therefore, caution should always be used when designing rms measuring systems which must deal with complex waveform amplitudes above 1 volt rms.

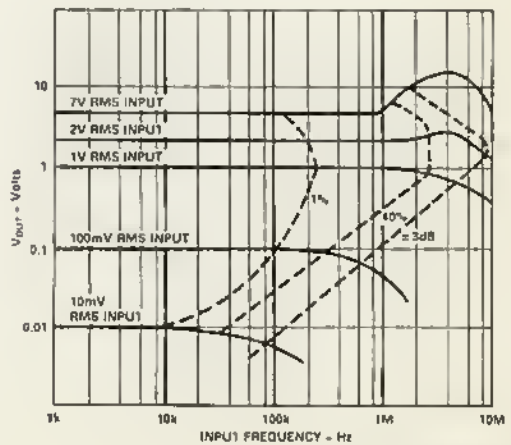


Figure 13. AD637 High Frequency Response

FILTERS AND AVERAGING

INTRODUCTION

RMS converters are capable of accurately measuring the rms value of both the dc and the ac components of an input signal. Unfortunately, as with all real (nontheoretical) measuring devices, inaccuracy needs some qualification or detailed explanation. It is, therefore, useful to understand the sources of these errors to optimize an rms converter's performance for a particular application, and as with all real systems, some design trade-offs are necessary.

AVERAGING AND FILTERING TIME CONSTANTS

There are two major design decisions required:

1) Choosing the averaging time constant
2) Choosing the post filtering time constant

The averaging time constant Y_1 will equal:

$$\tau_{IN}\,\text{SECONDS} = \frac{0.025\,\text{SECONDS}}{\mu F} \times C_{AV}$$

for a $1\mu F\ C_{AV}$ τ will equal:

$$\frac{0.025\,\text{SECONDS}}{\mu F} \times 1.0\mu F$$

$$= 0.025\,\text{SECONDS OR } 25\text{ms}$$

Since the averaging time is the time in which the rms converter "holds" the input signal during computation, it directly effects the accuracy of the rms measurement.

DC ERROR AND OUTPUT RIPPLE

Figure 14 shows the typical output waveform of an rms converter with a sinewave input applied. In reality, the ideal value ($V_{OUT} = V_{IN}$) is never actually achieved; instead, the output contains both a dc and an ac error component.

For an rms converter with negligible offset, scale factor, and linearity errors: the dc error component is the difference in dc volts between the average of the output signal (average E_o line of Figure 14) and the ideal output (ideal E_o). Mathematically, this equals:

$$\text{DC ERROR (IN \% OF READING)} = \frac{1}{0.16 + (6.4\tau_1{}^2F^2)}$$

$$\text{where } \tau_1 = 0.025\frac{\text{SECONDS}}{\mu F} \times C_{AV}$$

F = Input frequency in Hz

The ac component of output error is present in the form of an output ripple whose frequency is double that of the input signal (for symmetrical waveforms). The peak value of the output ripple equals:

$$\text{PEAK RIPPLE } C_{AV}\text{ ONLY (IN \% OF READING)} = \frac{50}{1 + (40\tau_1{}^2F^2)}$$

As a practical example, using the circuits of Figures 15 and 16:

An input frequency of 60Hz and $1\mu F\ C_{AV}$ will give a dc error of . . .

$$\frac{1}{0.16 + (6.4 \times (0.025)^2 \times (60)^2)} = 0.0687\%$$

The peak output ripple for these same conditions will equal . . .

$$\frac{50}{\sqrt{1 + (40 \times (0.025)^2 \times (60)^2)}} = 5.241\%$$

The ac error or ripple may be easily removed at the output of the converter by a simple low pass filter (see Figures 22 and 23). But, in contrast, the dc error is set by the averaging time constant *alone* and *cannot* be reduced by post filtering. This becomes apparent

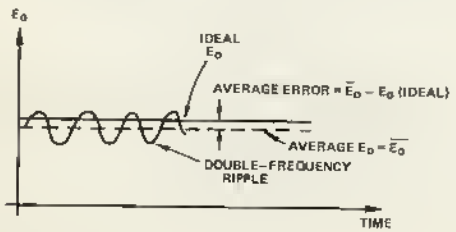


Figure 14. Typical Output Waveform for Sinusoidal Input

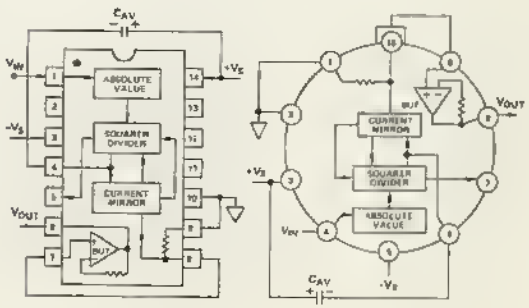


Figure 15. AD536A/AD636 Standard rms Connection

by noticing that even a perfectly averaged output that might be achieved by using a very large output filter (the average E_o line of Figure 14) still never approaches the ideal value.

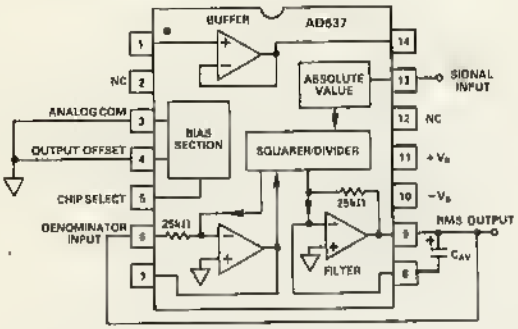


Figure 16. AD637 Standard rms Connection

Keep in mind that the dc error will be less than 0.2% of reading for sinewave inputs with frequencies greater than $1/\tau$ (for example $\geqq$40Hz for τ = 25ms) and that the error varies as $1/F^2$.

In practical terms, this means that as the input frequency doubles, the dc ERROR reduces to 1/4 of its original value and rapidly becomes insignificant as the input frequency is raised further.

Since there are two components of averaging error, (dc error and ripple) at the converter's output, the exact nature of the devices following it become important. For example, some applications are entirely or predominantly insensitive to output ripple: analog meter movements, and meters which have hardware or software averaging carried out within them are good examples. For such cases, only the MAGNITUDE of the dc error is important.

For other devices, such as digital meters without internal averaging, the dc and ac components both add to the uncertainty of the measurement with the maximum uncertainty or "averaging error", equal to the *peak* value of the output ripple plus the dc error.

THE STANDARD RMS CONNECTION

Figure 17 gives practical values of C_{AV} for various values of averaging error over frequency for the standard rms connections (no post filtering) of Figures 15 and 16. The standard rms connection has the advantage of requiring only one external component.

DESIGN CONSIDERATIONS – ERROR VERSUS RIPPLE

As previously stated, if the devices following the converter are ripple sensitive, the ripple must be reduced, optimumly *at least* below the level of the dc error.

A comparison of the left-hand bar to that of the dotted line of Figure 18 shows that the error due to the output ripple using a C_{AV} only is considerably larger than that due to the dc error. For example, the peak ripple at 50Hz is sixty-three times the level of the dc error when no post filter is used, i.e., 6.3% ripple versus 0.1% dc error (both specified in % of reading).

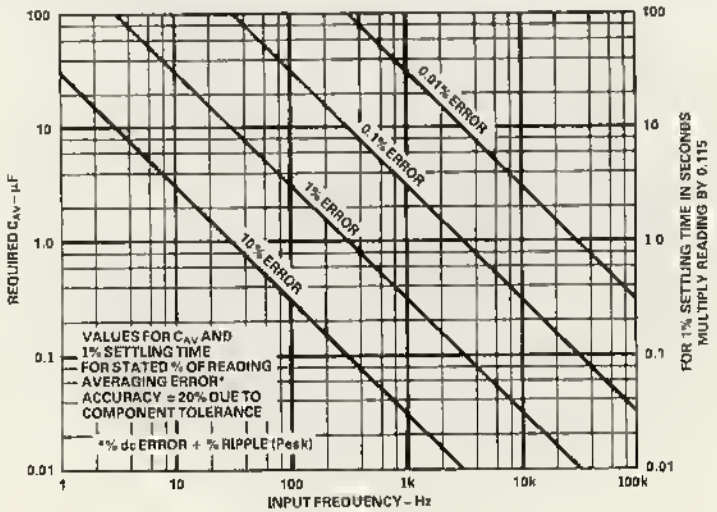


Figure 17. Error/Settling Time Graph for Use with the Standard rms Connection

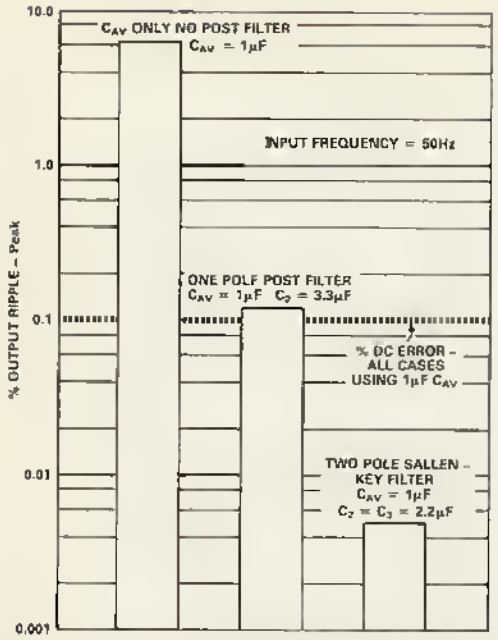


Figure 18. Comparison of the Level of dc Error to that of the Ripple Amplitude – AD536A/AD637 (for AD636 Multiply Values of C2 & C3 by 2.5)

This graph dramatically shows the effectiveness of a post filter in reducing overall averaging error. Note: when using C_{AV} alone, the output ripple constitutes over 99% of the total averaging error; for the one pole filter case using C_2 equal to 3.3 times C_{AV}, the ratio is close to 50/50, and for a 2 pole filter with C_2 and C_3 equal to 2.2 times C_{AV}, the dc error is the main source of error contributing to approximately 95% of the averaging error.

The addition of a single capacitor to the output of the rms converter (see Figures 22 and 23), in this case with a value of 3.3μF, will reduce the output ripple to 0.12%–almost fifty-three times. A two pole filter, shown by the right hand bar of Figure 18, reduces the ripple (and overall averaging error) still further. Of course, the 50Hz ripple could be reduced to the 0.1% level by increasing C_{AV} fifty-three times– to 53μF. Unfortunately, this not only gives values of C_{AV} that may be physically too large, but it creates another problem–excessively long averaging and settling time constants. (See the following section for an explanation of settling time.)

FILTERING VERSUS SETTLING TIME

Settling time is defined as the time required for an rms converter to settle to within a given percent of the change in rms level. The relationship between the value of C_{AV} and output settling time is set by the averaging time constant and varies 2 to 1 between increasing and decreasing input signals. Increasing input signals require 2.3 time constants to settle or:

$$ts = 2.3 \times (0.025 \frac{\text{SECONDS}}{\mu\text{F}} \times C_{AV})$$

to within 1% of the *change* in rms level. Decreasing signals require 4.6 time constants:

$$ts = 4.6 \times (0.025 \frac{\text{SECONDS}}{\mu\text{F}} \times C_{AV})$$

to within 1% of the *change* in rms level.

This translates into 57.5ms per μF C_{AV} for increasing signals and 115ms per μF for decreasing signals. For most applications, the 115ms per μF figure should be used, therefore providing the worst case settling time.

Note: The formulas, graphs, and computer programs in this application guide all establish the worst case (or decreasing amplitude) settling times.

Settling Time versus Input Level–AD536A and AD636 Only

In addition to the 2:1 difference in settling time for increasing and decreasing signals, the AD536A/

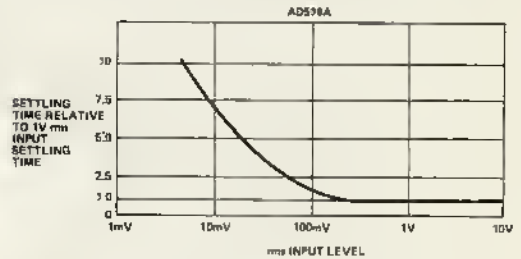


Figure 19. AD536A Settling Time vs. Input Level

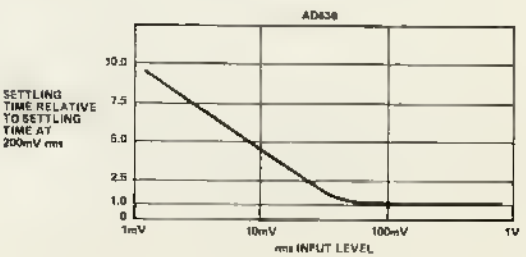


Figure 20. AD636 Settling Time vs. Input Level

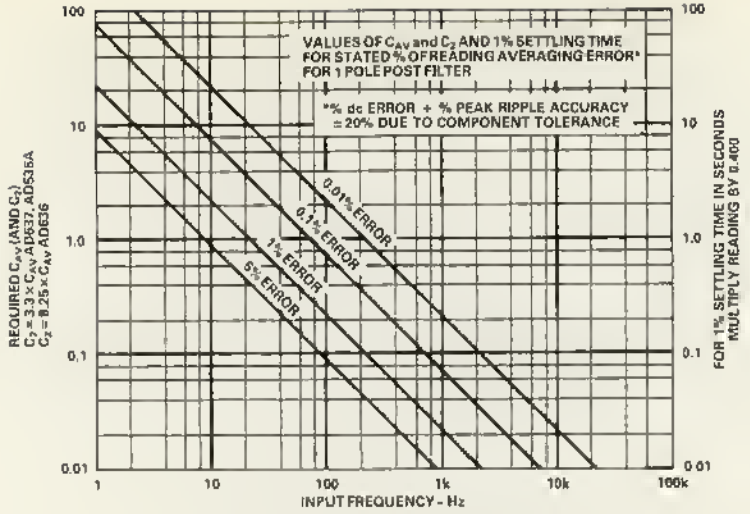


Figure 21. Error/Settling Time Graph for Use with 1 Pole Output Filter Connection

AD636 settling time will also vary with input signal level, increasing as the input level is reduced, as shown in Figures 19 and 20.

Note: The AD637 settling time is constant with input signal level, dependent only on the amount of C_{AV}.

Using A One Pole Output Filter to Reduce Ripple and Overall Settling Time

For the 53μF C_{AV} example, the time required for the output to settle to within 1% (of the change in rms level) would equal *5.3 seconds*! For most applications, its far better to pick a value of C_{AV} just large enough to give the desired maximum dc error at the lowest frequency of interest and use post filtering to remove the excess ripple. For the one pole post filter the best overall compromise between averaging error and settling time occurs with the value of C_2 equal to 3.3 times the value of C_{AV}. (Figure 21 gives recommended capacitance values using these ratios.) Settling time *does* increase with the addition of this extra capacitor, but the increase is much less than if ripple had been reduced using C_{AV} alone. For a one pole output filter, the total worst case settling time will equal the root sum squares of the averaging and filtering time constants.

$$ts = \sqrt{(4.6\tau_1)^2 + (4.6\tau_2)^2}$$

where

$$\tau_1 = 0.025 \frac{\text{SECOND}}{\mu\text{F}} \times C_{AV}$$

$$\tau_2 = 0.025 \frac{\text{SECOND}}{\mu\text{F}} \times C_2$$

For example: Using the circuits of Figures 22 and 23, a 1μF C_{AV} and a 3.3μF C_2 will give a total settling time of . . .

$$ts = \sqrt{(0.115)^2 + (0.3795)^2} = 0.39655 \text{ seconds}$$

or 396.5ms

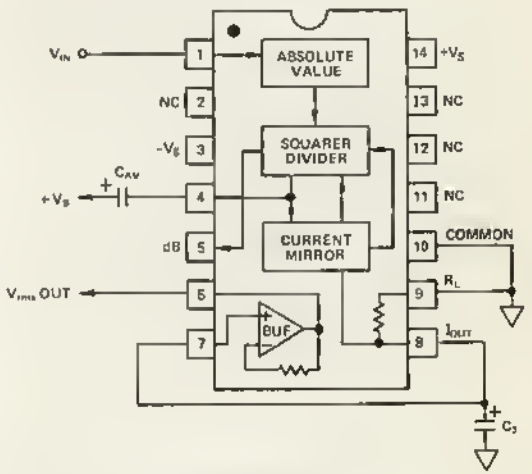


Figure 22. AD536A/AD636 with a 1 Pole Output Filter

The total 1% settling time for this example is only one thirteenth of that required for a 53μF C_{AV} using the standard rms connection, yet the one pole filter provides the same reduction in output ripple.

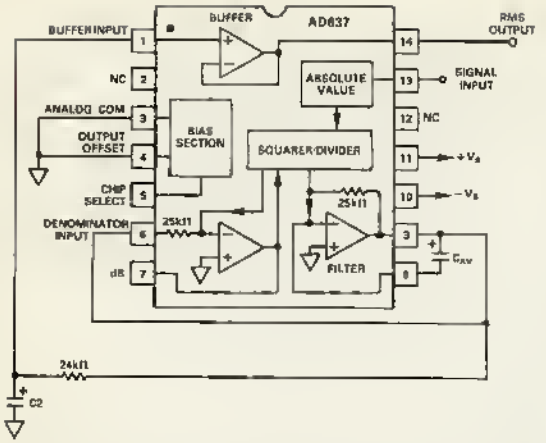


Figure 23. AD637 with a 1 Pole Output Filter

The formula for computing output ripple using the one pole filter circuits of Figures 22 and 23 is:

$$\%\ \text{ripple} = \frac{50}{\sqrt{1 + 40\tau_1^2 F^2}} \times \frac{1}{\sqrt{1 + (4\pi F)^2 (\tau_2)^2}}$$

where $\tau_1 = 0.025 \frac{\text{SEC}}{\mu\text{F}} \times C_{AV}$

$$\tau_2 = 0.025 \frac{\text{SEC}}{\mu\text{F}} \times C_2$$

F = Input signal frequency

Note: For automatic computation of error, ripple, and settling time using the Apple II Computer, see Appendix C.

Settling Time Approximations When Using a Post Filter

Referring to the one pole filter example: notice that when the rms converter is followed by a post filter, in this case with a recommended time constant 3.3 times that of the averaging section, the post filter dominates the overall settling time of the circuit. This effect also takes place when using a two pole output filter in which each section has a time constant 2.2 times (or more) that of the averaging section. Therefore, when using a post filter, the total settling time may be approximated to within 5% error by determining the post filter settling time alone.

For a one pole filter case using a 1μF C_{AV} and a 3.3μF C_2, ts of the output filter will equal: 0.025 SECONDS/μF times 3.3μF times 4.6 time constants = 397.5ms. Note how close 397.5ms is to the *exact* figure of 396.5ms which was previously calculated by finding the square root of the sum of squares!

Table 3 shows the basic formulas which determine the required settling time constants for the rms section to settle to within various percentages of the new rms level when undergoing a step change in input level. The values in brackets are those of a linear RC filter. As shown by the table, there is a consistent two to one difference in settling time between increasing and decreasing signals in the averaging section of the rms converter.

THE TWO POLE OUTPUT FILTER

Referring again to Figure 18, a further reduction in output ripple and, therefore, overall averaging error may be achieved by using one of the two pole sallen-key filters shown in Figures 24 and 25. The resistor and capacitor ratios in these filters were chosen to provide a Butterworth or flat amplitude versus frequency response.

Figure 18 shows that with the two pole output filter,

	For Increasing Amplitudes	For Decreasing Amplitudes
Basic Formulas	$\Delta V\sqrt{1-e^{-T/RC}}$	$\Delta V\sqrt{e^{-T/RC}}$
Settling Time to Within Stated % of New rms Level		
1%	2.0τ (4.6τ)	4.6τ (4.6τ)
0.1%	3.1τ (6.9τ)	6.9τ (6.9τ)
0.01%	4.2τ (9.2τ)	9.2τ (9.2τ)
( )Settling Times for Linear RC Filter		

Table 3. Number of RC Time Constants (τ) Required for AD536A, AD636, AD637 rms Converters to Settle to Within Stated % of Final Value

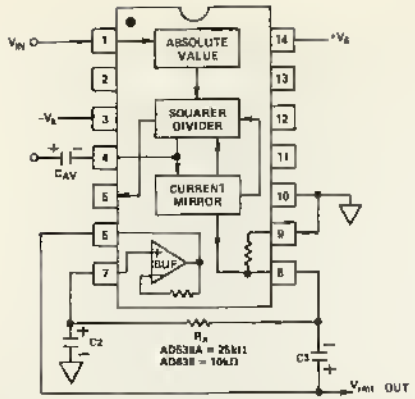


Figure 24. AD536A/AD636 with a 2 Pole Output Filter

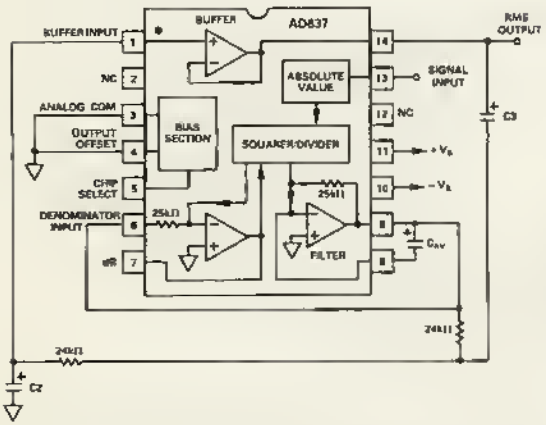


Figure 25. AD637 with a 2 Pole Output Filter

the predominant component of averaging error is the dc error, in fact, in this case, the dc error is twenty times greater. The % ripple output of the two-pole sallen-key filter will equal the ripple input to the filter (from the rms converter output) times the transfer function of the sallen-key filter.

$$\%\ \text{ripple} = \frac{50}{\sqrt{1 + 40\,\tau^2 F^2}} \times \frac{\left(\frac{1}{\tau_2}\right)^2}{\sqrt{\left[\left(\frac{1}{\tau_2}\right)^2 - (4\pi F)^2\right]^2 + \left(\frac{8\pi F}{\tau_2}\right)^2}}$$

where: $\tau_1 = 0.025 \dfrac{\text{SECONDS}}{\mu\text{F}} \times C_{AV}$

where: $\tau_2 = 0.025 \dfrac{\text{SECONDS}}{\mu\text{F}} \times C_2$

$C_2 = C_3$

F = Input signal frequency in Hz

For automatic computation of dc error, ripple, averaging error, and settling time using the Apple II Computer, See Appendix C. As with the other rms connections, averaging error may be determined via the computer program, by using the formulas directly, or in this case, by referring to Figure 26.

The *exact* 1% settling time (worst case) for the two pole post filter circuit equals the root sum squares of

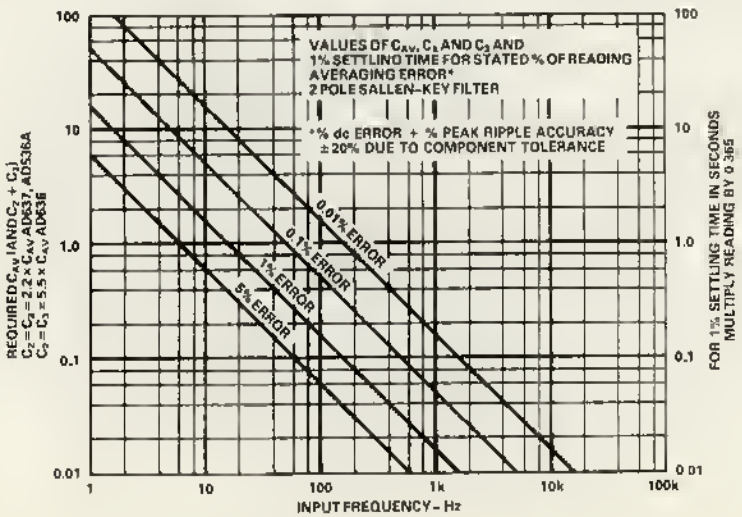


Figure 26. Error/Settling Graph for Use with 2 Pole Output Filter

the settling time due to C_{AV} plus the settling times of each pole of the filter. That is:

$$\text{ts two pole output filter} = \sqrt{(4.6\tau_1)^2 + (4.6\tau_2)^2 + (4.6\tau_3)^3}$$

where: $\tau_1 = 0.025 \frac{\text{SECONDS}}{\mu\text{F}} \times C_{AV}$

where: $\tau_2 = 0.025 \frac{\text{SECONDS}}{\mu\text{F}} \times C_2$

where: $\tau_3 = 0.024 \frac{\text{SECONDS}}{\mu\text{F}} \times C_3$

Note: As with the one pole filter, the circuit settling time may be very closely approximated (to within 5%) by calculating the settling time of the post filter alone. For a two pole filter, this equals 1.4 times the time constant of either section times 4.6 time constants (for $C_2 = C_3$). Using a 1μF C_{AV}–2.2μF C_2, C_3 example, the approximate circuit settling time to 1% will equal: ts = 1.4 × 0.025 SECOND/μF × 2.2μF × 4.6 = 354.2ms.

DETERMINING THE COMBINED ERROR OF THE RMS MEASURING SYSTEM

The total worst case error of an rms circuit will be the sum of all its individual errors. To closely approximate this *combined* error, first decide on whether or not an output filter is needed: then select an appropriate value of C_{AV} (and C_2 and C_3 if they are used). Go to the appropriate graph and find the averaging error at the lowest frequency of interest. Add this to the "total error internal (or external for an externally trimmed circuit) trim" spec. The combined error is then the maximum *worst case* error the system will produce, even though in most cases performance will be better. (In particular, performance will always improve as the input frequency increases.)

Note: If all of this sounds confusing, try this cookbook approach:

Select the "J" grade part, take its "total error" spec, and add 1% to it. If this gives too great a combined error, go to the "K" grade part or provide for external trimming and use that improved spec. Go to the one pole post filter graph and find the lowest frequency of interest. Then find the value of C_{AV} from where the 1% averaging error line intersects with the frequency line. (If settling time is *not* a problem, use the 0.1% averaging error lines on the charts.)

Once the value of C_{AV} is known, C_2 is found by multiplying the value of C_{AV} by: 3.3 for the AD637 and AD536A, or 8.25 for the AD636. Total settling time for the system is the point on the right hand vertical axis directly across from the C_{AV}, C_2 scale. If settling time is found to be too great, it may be reduced (approximately 30%) by using a two pole post filter. For this case, use the two pole filter graph, find the new values for C_{AV}, C_2, and C_3 and the corresponding settling time for the circuit.

USING THE INTERNAL BUFFER AMPLIFIER TO ISOLATE THE FILTERING CIRCUIT

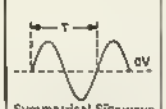
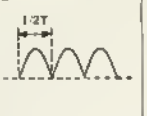
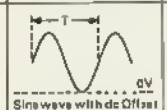
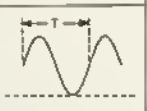
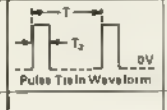
The primary use of the AD536A/AD636 internal buffer amplifier is as an output buffer in its standard output configuration. The obvious advantage of using an output buffer is to isolate the filtering circuit (capacitor C_2 and internal load resistor R_L), from external loads being driven by the rms converter (see Figure 24). Unless these loads are *very* high impedance, they will adversely effect both the scale factor accuracy and the filtering performance of the rms converter. The $10^8\Omega$ buffer input impedance allows the output filter to operate independent of any external loading effects.

Note: Since the AD637 has a low impedance output, its internal buffer amplifier may not be required. For design considerations concerning the use of either the AD536A or AD636 with its internal buffer amplifier serving as an input buffer, see Appendix B.

THE EFFECTS OF THE SYMMETRY, DC OFFSET, AND DUTY CYCLE OF INPUT WAVEFORMS ON THE REQUIRED VALUE OF C_{AV}

The selection of averaging capacitor value given in the previous sections was based on the input signals being symmetrical (sine, triangle, or square) waveforms. If asymmetrical waveforms or low duty cycle pulse trains are applied to the input of an rms, converter, the total averaging time (and, therefore, the value of C_{AV}) required will increase.

The reason for this increase becomes apparent by referring again to Figure 32. As shown by the figure, the averaging takes place at the C_{AV} terminal, a point in the circuit *after* the absolute value circuit. The absolute value circuit full wave rectifies the input signals–effectively doubling that frequency provided that the input waveform is symmetrical. It is, therefore, important to consider the input waveform as it appears after full wave rectification when deciding on the value of C_{AV}. Table 4 illustrates this point and gives averaging time constant ratios for various types of input waveforms. In addition, practical component values for 60Hz input signals are also specified.

	Input Waveform and Period	Absolute Value Circuit Waveform and Period	Minimum R × C_{AV} Time Constant	Recommended C_{AV} and C2 Values for 1% Averaging Error at 60Hz with T = 16.6ms			1% Settling Time
				C_{AV} as Calculated	Recommended Standard Value C_{AV}	Recommended Standard Value C2	
A	 Symmetrical Sinewave		1/2T	0.33µF	0.47µF	1.5µF	701ms
B	 Sinewave with dc Offset		T	0.68µF	0.82µF	2.2µF	225ms
C	 Pulse Train Waveform		$10(T - T_2)$	5.88µF for $T_2 = 0.1T$	6.0µF	22µF	2.67sec
D			$T0(T - 2T_2)$	5.31µF for $T_2 = 0.1T$	5.6µF	16µF	2.17sec

VALUES ARE SPECIFIED FOR AD536A AND AD637. FOR AD636 MULTIPLY C2 VALUES BY 2.5.

Table 4. A "Cookbook" Capacitor Selection Chart for Various Input Waveforms

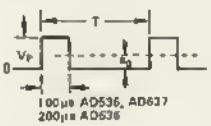
Note: For frequencies other than 60Hz, capacitance values may simply be ratioed (i.e., 30Hz = 2 × 60Hz values, 120Hz = 1/2 60Hz values) or calculated using the new R × C_{AV} averaging time constants.

Table 5 gives practical component values for SCR type input waveforms with frequencies of 50Hz and 60Hz.

ERROR VERSUS CREST FACTOR

AD536A

Figure 27 provides % reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 10 (1 volt peak amplitude). A rectangular pulse train (pulse width 100µs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce the various crest factors while maintaining a constant 1 volt rms input amplitude.



η = DUTY CYCLE = $\frac{100\mu s}{T}$ or $\frac{200\mu s}{T}$

$CF = 1/\sqrt{\eta}$

e_{in} (rms) = 1 Volt rms – AD536A, AD637
200MV – AD636

Input Frequency and Period	Absolute Value Circuit Waveform and Period	C_{AV} Value			C_2 Value (3.3 × C_{AV})			1% Settling Time
		Calculated Value for 10 Time Constants	+20% to Provide for Component Tolerance	Closest Standard Value	Calculated Value for 10 Time Constants	+20% to Provide for Component Tolerance	Closest Standard Value	
60Hz 16.67ms		3.2µF	3.84µF	4.7µF	10.56µF	12.67µF	15.0µF	1.31sec
50Hz 20ms		4.0µF	4.8µF	5.6µF	12.2µF	15.8µF	15.0µF	1.84sec

VALUES GIVEN FOR TPOLE POST FILTER CONNECTION AD536A, AD637 FOR AD636 MULTIPLY C_2 VALUE BY 2.5

Table 5. Capacitor Selection Chart for SCR Input Waveforms for a Maximum of 1% Worst-Case Averaging Error

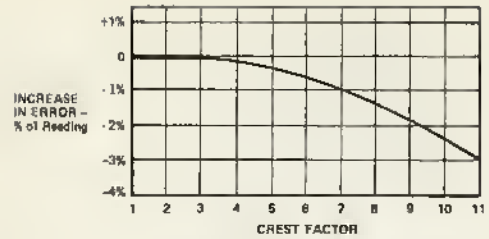


Figure 27. AD536A Error vs. Crest Factor

AD636

Figure 28 shows the error versus crest factor for the AD636 rms converter with a 200mV rms input signal applied. Crest factor range for the AD636 is from 1 to 7 (1.4 volts peak amplitude). The pulse width in this case was 200μs.

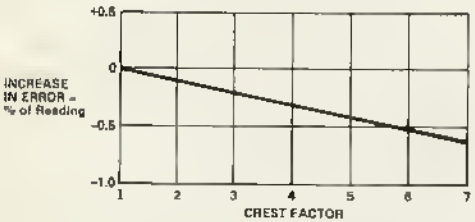


Figure 28. AD636 Error vs. Crest Factor

AD637

As displayed by Figure 29, the error versus crest factor of the AD637 will vary within the shaded portion of the graph. This variation is due to component tolerances in each chips internal compensation network. Fortunately, the overall variation is quite small.

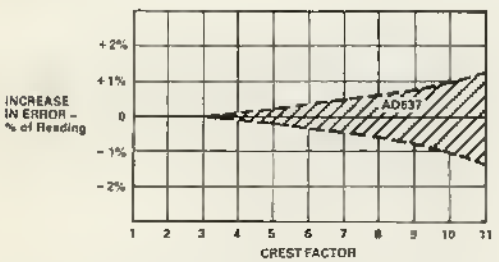


Figure 29. AD637 Error vs. Crest Factor

SINGLE SUPPLY OPERATION

AD536A

Rather than using symmetrical power supplies to operate the AD536A, a single polarity supply as low as +5 volts may be used instead. This requires biasing the AD536A common terminal (pin 10) above ground as shown in Figure 30. The ratio of two resistors, R_1 and R_2 form a voltage divider between $+V_S$ and ground. Choosing the correct bias voltage for the common terminal is a trade-off between the maximum positive and the maximum negative input voltage the AD536A can tolerate without clipping. For example, as resistor R_2 is made larger, pin 10 is effectively raised more above ground. This will increase the maximum negative input voltage of the AD536A while at the same time decreasing the maximum positive input voltage the rms converter can handle. The values of resistors R_1 and R_2 in Figure 30 were selected to give the best overall operation using a +15 volt supply, however, pin 10 should be at least +2 volts above ground for correct operation. The AD536A common pin requires less than 5μA of input current, therefore, the values of resistors R_1 and R_2 can be chosen so that:

$$\frac{V_{SUPPLY}}{R_1 + R_2} = 50\mu A$$

or 10× the common pin current. This permits adequate voltage stability on the common pin while still minimizing overall power consumption.

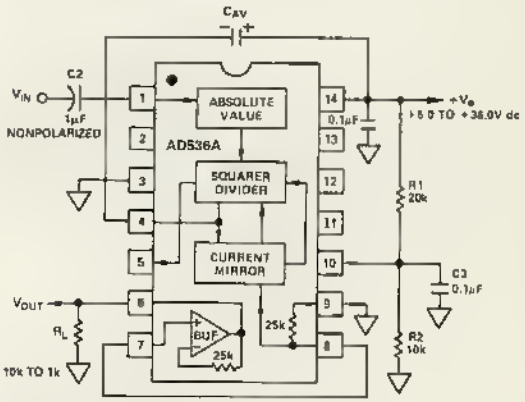


Figure 30. AD536A Single Supply Connection

AD636

The AD636 low power rms converter may also be operated from a single power supply, in this case between +5.0V dc and +24.0V dc. The same design trade-offs apply to the AD636 as to the AD536A when choosing the optimum values for resistors R_1 and R_2, although since the AD636 was optimized to operate from unequal supplies (+3.0, −5.0V dc), the ratio of the two resistors will be different for the two devices. The values for resistors R_1 and R_2 in

Figure 31 were chosen for the best overall performance using a 9 volt battery (for examples of battery operation, see dB Meters Section).

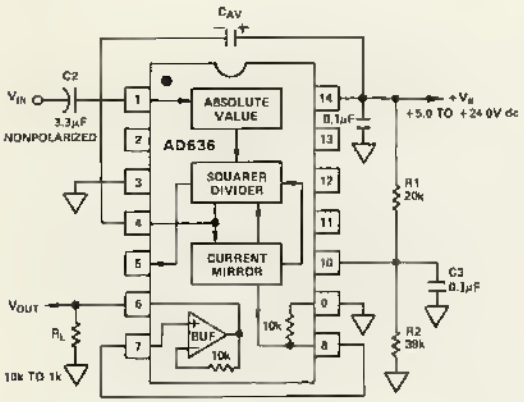


Figure 31. AD636 Single Supply Connection

AD637

The AD637 has its output voltage derived via an inverting low pass filter which does provide output buffering, however, the operational amplifiers in this filter stage will not operate down to the negative supply (as will the current mirror in the AD536A/AD636). The AD637 *can* be operated from a single supply voltage but only if its output voltage does not have to be less than 2 volts above the negative supply. Therefore, you may bias the AD637 above ground using equal value resistors (R1 & R2 with typical values of approximately 15kΩ); this allows single supply operation from power supplies between +5 volts and +36 volts dc using the same scheme shown in Figures 30 and 31. Please note: Because the filter amplifier's common pin cannot be separated from the rms converter common, the AD637 output MUST be referenced to its common pin (pin 3), NOT TO GROUND.

THE DECIBEL OUTPUT PROVISION

Basic Operating Principles

As shown by Figure 32, the dB output function originates in the squarer/divider section of the AD536A/AD636. Figure 33 shows a portion of this section redrawn to illustrate dB operation. Although component values vary, this basic scheme is common to the AD536A, AD636, and the AD637 rms converters.

The feedback current, I_3, proportional to the rms value of the input signal, is applied to the input of A_3. Transistor Q_3, in conjunction with amplifier A_3, forms a logarithmic amplifier whose output *voltage* is proportional to the natural logarithm of *current* I_3. The output of A_3, which is the V_{BE} of Q_3, is equal to:

$$V_{BE_{Q3}} = \frac{-kT}{Q} \text{ LN } \frac{I_3}{I_{ES}}$$

where $\frac{kT}{Q}$ is the thermal voltage of Q_3's base emitter junction and I_{ES} is Q_3's emitter saturation current.

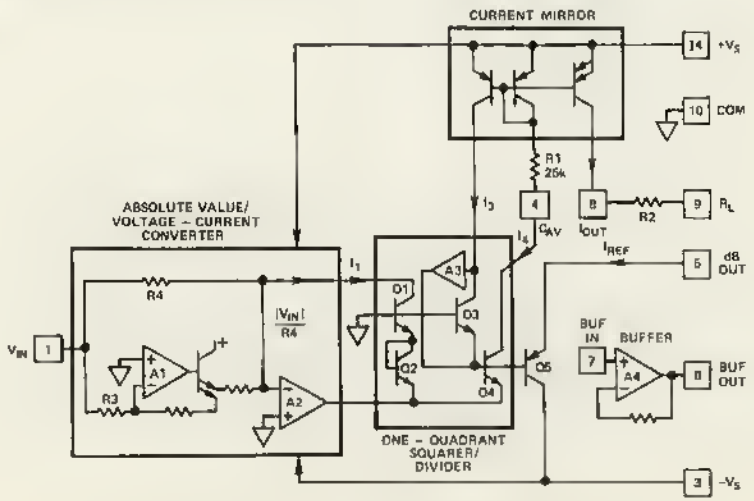


Figure 32. AD536A/AD636 Simplified Schematic

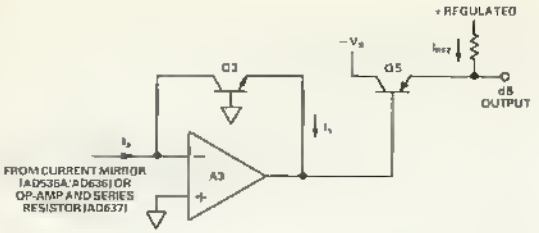


Figure 33. A Simplified Schematic of the dB Output Circuitry Common to the AD536A, AD636 and AD637 rms Converters

This output has two thermal or temperature related drift causing elements. One is a scale factor drift caused by the kT/Q term which is approximately equal to 0.33% drift per degree centrigrade *at* 25°C (3300ppm/°C). The second drift term is an offset drift due to the I_{BS} of transistor Q_3. This offset varies with temperature approximately 2mV/°C.

The decibel is based on the log of the ratio of two signals, or

$$dB = 20 \text{ LOG } \frac{IA}{IB}$$

Since two currents are needed, a second current I_{REF} is introduced via a second transistor Q_5.

Q_5 performs several functions necessary to dB operation:

1. It performs the required division function by subtracting the logs of the two currents I_3 and I_{REF}.
2. By having its V_{BE} subtracted from the V_{BE} of Q_3, Q_3's junction offset and offset voltage drift over temperature characteristics are corrected.
3. Q_5 provides the necessary current buffering for the dB output pin.

The output voltage at the dB output terminal (via Q_5) equals:

$$dB \text{ OUTPUT} = (V_{BEQ3}) - (V_{BEQ5})$$

$$\frac{-kT}{q} \text{ LN } \frac{I_3}{I_{REF}} \text{ U}$$

Note: U accounts for the ratio of the emitter saturation currents of Q_5 and Q_3 and also for the imperfect tracking of the V_{BE} of Q_5, a PNP transistor, with the V_{BE} of Q_3, an NPN transistor. Fortunately, for most practical applications this tracking error is negligible, as long as I_{REF} is used as a reference level *AND NOT* as a signal input.

The dB output produces an output voltage approximately equal to 3mV/per dB change in I_3; it needs to be scaled and temperature compensated to be useful for most applications, (temperature compensation is required because although the offset portion of Q_3's drift has been subtracted out the 3300ppm/°C temperature drift due to $\frac{kT}{q}$ still remains). Succeeding sections will cover these requirements in detail.

AD536A/AD636 Temperature Compensation

With a temperature coefficient of 0.03dB/°C, the total error for the dB output would be ±0.3dB for a ±10°C variation in operating temperature. In many cases, this accuracy is satisfactory. However, for more critical applications the addition of an external temperature compensating resistor is necessary.

The circuit of Figure 34 provides temperature compensation by using the averaged TC of two resistors in series to develop the desired 3300ppm. These resistors, placed between the dB output pin and the summing junction of the AD741 scale factor amplifier, change the scale factor of the circuit when temperature variations occur.

The 1kΩ +3500ppm/°C TC resistor in series with a 60.4Ω 1% metal film resistor together form a 1.06kΩ +3300ppm resistor, the exact TC needed. The metal film resistor is ±50ppm and may be considered "zero" TC compared with the +3500ppm/°C resistor. The metal film resistor therefore degrades or reduces the TC resistors +3500ppm/°C by the ratio of their resistances, in this case by 6.04%.

$$\frac{60.4\Omega}{1000\Omega} \times 100\% = 6.04\% \quad 3500\text{ppm} \times 0.94$$

$$(94\%) = 3290\text{ppm/°C}$$

AD637 Temperature Compensation

This scheme, shown by Figure 35, is basically the same circuit as Figure 34 except that it requires an 820kΩ resistor connected between the rms output, pin 9, and the summing junction of the AD741 output amplifier. This resistor compensates for errors in the dB circuit for input levels above 1V rms. In both circuits, the output amplifier gain is set to give a 100mV output per dB change in input level.

This circuit out performs that of Figure 34 providing a −3dB bandwidth of 4MHz with a 1V rms input level. It operates over a 70dB range from +10dB to −60dB ±2.5dB with a 0dB reference level of 1 volt

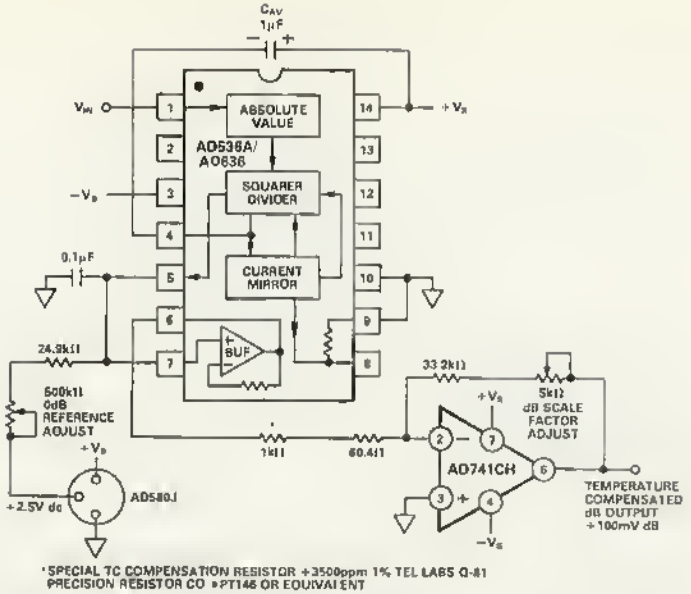


Figure 34. AD536A/AD636 Temperature Compensated dB Output Circuit

rms. The 0dB reference point may be varied ± 10dB from the nominal 1 volt level by using the 500kΩ 0dB adjust trimpot, however, if higher resolution is required (using 0dB = 1 volt rms) a 100kΩ trimpot may be substituted.

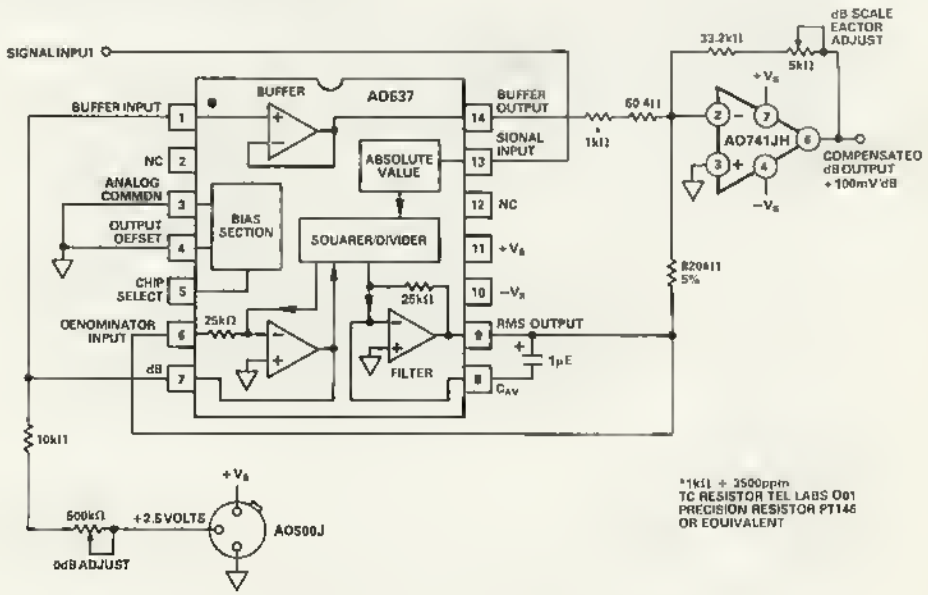


Figure 35. AD637 Temperature Compensated dB Circuit

SECTION III

RMS APPLICATIONS CIRCUITS

SIGNAL PROCESSING
AN RMS–AGC AMPLIFIER

Introduction

One of the major problems facing the designer of function generators is how to maintain a constant output level with variations in waveform, duty cycle, and frequency. Many conventional AGC (Automatic Gain Control) amplifiers suffer from poor performance, usually a restricted dynamic range and inadequate frequency response. These amplifiers usually provide a constant "average" output level, or instead employ a peak limiting scheme which controls the maximum "peak" output level. In many applications, it is more useful to have a constant rms output level from an AGC amplifier.

The rms-AGC amplifier presented here has many audio uses and will provide a virtually constant rms output voltage over an input variation of greater than 40dB (see Figure 37).

Circuit Description

As shown in Figure 36, the voltage output from the AD534 multiplier is converted to its dc equivalent voltage by an AD536A rms to dc converter. Capacitor C_4 is the rms converter's averaging capacitor. The output voltage from the converter is compared to a fixed reference voltage provided by an AD580 bandgap reference. An AD741 is used as an integrator/comparator amplifier whose output voltage sets the gain of the AD534 multiplier. The AD741 amplifies the difference between the rms out-

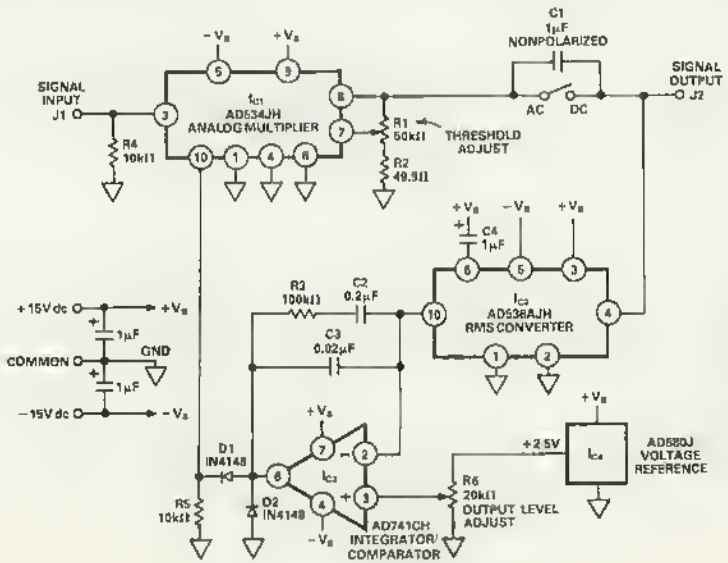


Figure 36. An rms AGC Amplifier

put level from the AD536A and the preset dc voltage derived via the output level control, R_6. This amplified output voltage appears at pin 6 of the AD741 after a delay time set by the series/parallel RC combination of C_2C_3 and R_3 in the operational amplifier's feedback loop. The two diodes, D_1 and D_2, keep the output of the AD741 from going negative; this would change the phase of the control loop by 180°.

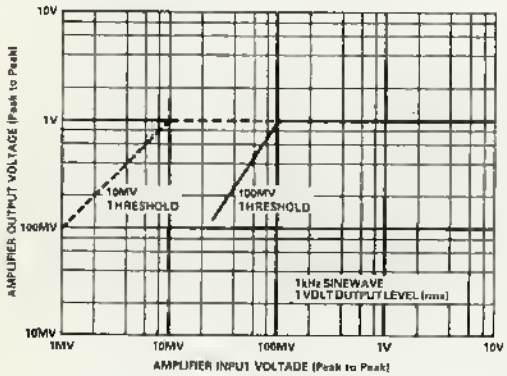


Figure 37. Input vs. Output – rms AGC Amplifier

Performance Data

All measurements were taken with 300mV threshold and 1 volt output level. Note: Different types of waveforms may have widely varying crest factors; consequently, even though they have the same rms level, their peak values may be quite different. Since amplifier overload occurs due to the peak values of the signal waveforms, all voltage specifications in this circuit, and in the audio AGC amplifier, are given in peak to peak.

Input Range: 300mV to 28 volts (40dB)
Frequency Response: dc to 400kHz @ 300mV input, dc to 1MHz @ 1 volt input.
Signal to noise ratio: 65dB
Attack/hold-in time: 100ms

AUDIO PROCESSING
AN AUDIO RMS – AGC AMPLIFIER

Introduction

Here is an audio amplifier incorporating a smooth sounding automatic gain control with a gradual acting threshold level. This circuit eliminates the usual audible "thump" of most compressor amplifiers by slowly incorporating the AGC action (Figure 39).

This design offers a great amount of flexibility featuring: controls for input range, degree of compression, and output level.

Circuit Description (see Figure 38)

The audio input signal, adjusted by R_4, is amplified by an AD544 operational amplifier operating with a gain of 21. The AD544 voltage output drives the controlled gain stage, an AD534 analog multiplier. The

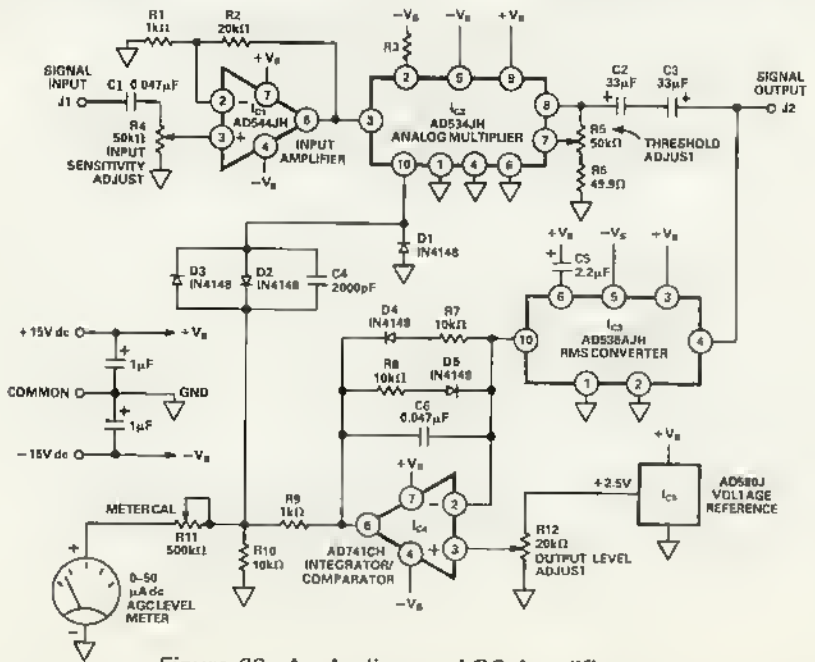


Figure 38. An Audio rms AGC Amplifier

2.49kΩ resistor in series with pin 2 of the multiplier may be varied from 2kΩ to 3kΩ for the best compromise between bandwidth and signal to noise ratio. This resistor sets the trade-off of gain versus bandwidth of the analog multiplier.

The multiplier's output is ac coupled to the signal output jack and to an AD536A rms – dc converter. The rms converter's current output drives a comparator/amplifier, IC_4, which acts as a current to voltage converter. The comparator's output, a positive voltage, is *decreased* by the rms converter's output, reducing the gain of the multiplier. The comparator's threshold point is prevented from being too abrupt by resistor diode networks, D_4/R_7 and D_5/R_8. The attack/release times of the circuit are determined mainly by capacitors C_5, C_6 and resistor R_7 and to a lesser extent, resistor R_8. Diodes D_1, D_2, and D_3 prevent latch-up of the multiplier by voltage transients. The degree of AGC action is monitored by the 0-50μA analog meter.

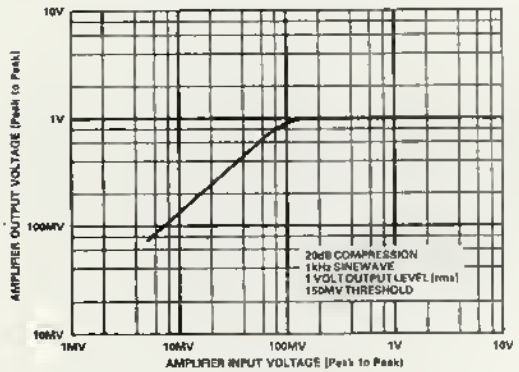


Figure 39. Input vs. Output – Audio rms AGC Amplifier

Performance Data
All voltages are specified peak to peak

Input range 150mV to 10 volts
Output level range variable 0.5 to 2.5 volt p-p
Compression variable from 0dB to 26dB
Threshold level ± 150mV to 1.6 volts

Frequency Response
10dB Compression
50Hz to 65kHz with 0.5V p-p input
50Hz to 100kHz with 1.0V p-p input
70Hz to 160kHz with 1.65V p-p input

20dB Compression
70Hz to 75kHz with 0.5V p-p input
70Hz to 120kHz with 1.0V p-p input
100Hz to 160kHz with 1.5V p-p input
With 1 volt p-p input and 1 volt p-p output level
attack time 250ms, release time 80ms
Signal to noise ratio
10dB compression 51dB, 20dB compression 45dB
Optimum output level 1 volt p-p
Total harmonic distortion 0.30%

To adjust the amplifier, first apply a 1 volt peak to peak sinewave at 1kHz to the input jack J_1. Adjust R_4 for a 2.5 volt peak to peak sinewave at the input of the multiplier, pin 3 of IC_2. Adjust R_5 to midposition. Next, adjust R_{12}, the output level control, for the desired output level, nominally 1 volt peak to peak. Adjust R_5 again, this time for the degree of compression desired. Trimpot R_{11} adjusts the output level meter's amplitude. Care should be taken when using the AGC amplifier to insure that the input is not overloaded (to avoid clipping the signal).

INSTRUMENTATION

RMS DIGITAL PANEL METERS (DPMs)

A LOW COST TRUE RMS DIGITAL PANEL METER

This low cost DPM features direct-reading true rms, a high impedance buffered input, four input ranges, and a minimum number of components. The DPM operates from a single 5 volt power supply requiring a total current of 100mA.

The input circuit of the device consists of a 10 meg ohm input attenuator with switch S_1 selecting the desired full scale input range. Capacitor C_5 ac couples the input of the rms converters internal buffer amplifier (pin 7 of the AD536A) with resistor R_8 and diodes D_1 and D_2 providing input circuit protection. The output of the buffer, pin 6, is ac coupled to the rms converter input, pin 1. Resistor R_5 provides a "bootstrapping" return path for the buffers input bias current, however, it does not effect the DPMs input impedance because the buffer is a unity gain follower, and pins 1 and 7 are at the same potential (see Appendix B). Resistor R_9 serves as a load resistor for the output of the buffer amplifier while resistors R_6 and R_7 provide a "floating" ground allowing single supply operation. Capacitor C_4 keeps the AD536A common, pin 10, at ac ground.

The output from the rms-dc converter (pin 8 of the AD536A) is low pass filtered by capacitor C_6; it then drives an AD2026 DPM. The rms meter's offset and

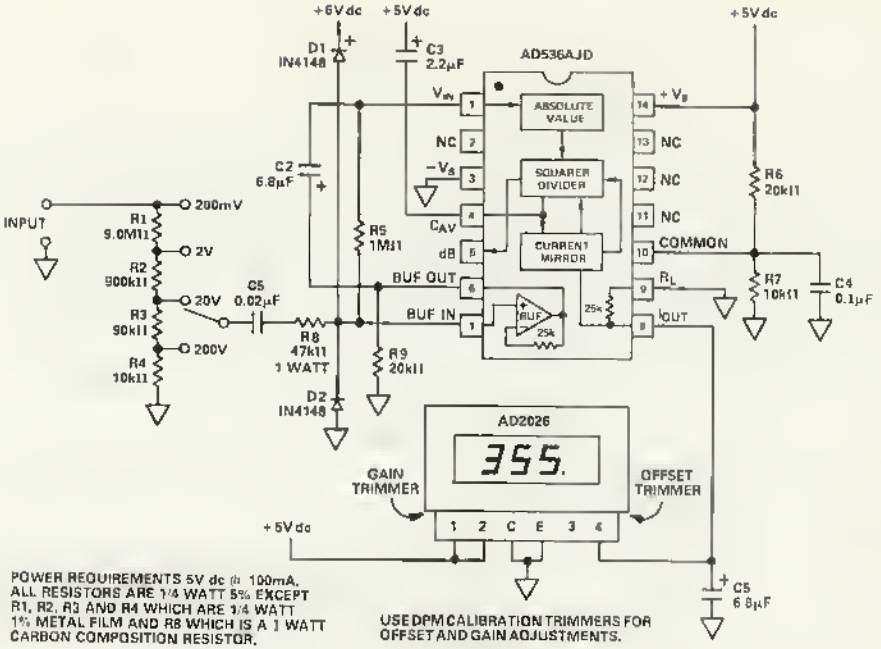


Figure 40. A Low Cost True-rms DPM

scaling adjustments are made using the DPM's internal calibration trimmers.

An ac line-powered version of the AD2026 is available which will permit this circuit to operate from power supplied by the DPM itself, thus eliminating the need for an external 5 volt power supply.

A PORTABLE HIGH IMPEDANCE INPUT RMS DPM AND dB METER

This high quality DPM/dB meter requires only two integrated circuits, their support circuitry, and a liquid crystal display.

As in the low cost DPM, the voltage input to the portable DPM runs through a 10 meg ohm input attenuator to pin 7 of the AD636. The buffer output, pin 6, is ac coupled to the rms converter's input, pin 1. Resistor R_6 provides a "bootstrapped" circuit to keep the input impedance high. The output from the rms converter is selected by the linear/dB switch; selecting pin 8 for linear, pin 5 for dB. The selected output travels from the linear/dB switch through low pass filter R_{15}, C_6 to the DPM chip's input. (The DPM chip is a 7106 type A/D converter.) The AD589 provides a stable 1.2 volt reference voltage which supplies the calibration circuitry.

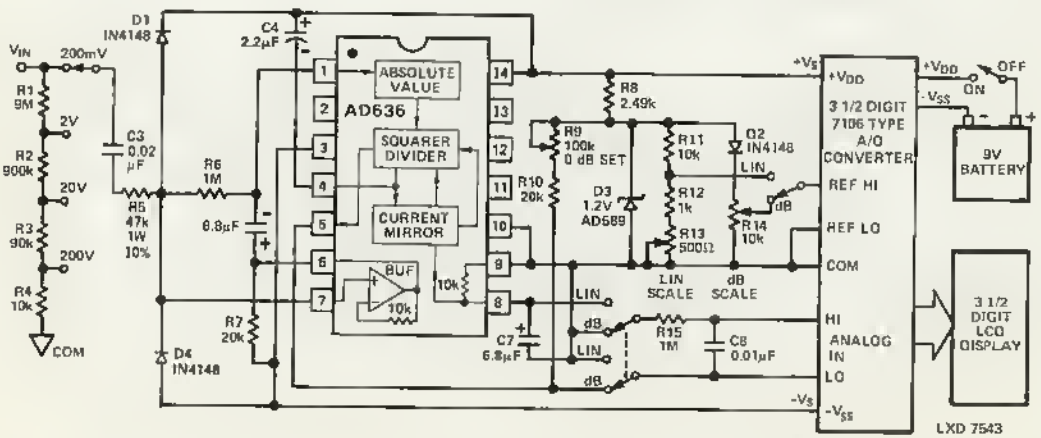


Figure 41. A Portable, High Z Input, rms DPM and dB Meter

To calibrate the meter, first adjust trim potentiometer R_9 for the 0dB reference point; next, set R_{14} for the dB scale factor, and finally, adjust R_{13} to set the linear scale factor. The total current consumption of the portable DPM is typically 2.9mA from a standard 9 volt transistor radio battery. This circuit utilizes the AD636 low power rms converter to extend battery life and to provide a 200mV full scale sensitivity. The AD636 gives better accuracy and bandwidth at 200mV rms inputs than the AD536A (the AD536A would require a gain of 10 preamplifier to achieve similar results at these levels.)

A LOW POWER, HIGH INPUT IMPEDANCE dB METER

Introduction

The portable dB meter circuit featured here combines the functions of the AD636 rms converter, the AD589 voltage reference, and a μA776 low power operational amplifier. It is also inexpensive, approximately $25.00. This meter offers excellent bandwidth and superior high and low level accuracy while consuming minimal power from a standard 9 volt transistor radio battery.

In this circuit, the built-in buffer amplifier of the AD636 is used as a "bootstrapped" (see Appendix B) input stage increasing the normal 6.7kΩ input Z to an input impedance of approximately $10^{10}\Omega$.

Circuit Description

The input voltage, V_{IN}, is ac coupled by C_4 while resistor R_8, together with diodes D_1 and D_2, provide high input voltage protection.

The buffer's output, pin 6, is ac coupled to the rms converter's input (pin 1) by capacitor C_2. Resistor R_9 is connected between the buffer's output, a Class A output stage, and the negative supply to increase the buffer amplifier's negative output swing (see Appendix B). Resistor R_1 is the amplifier's "bootstrapping" resistor.

With this circuit, single supply operation is made possible by setting "ground" at a point between the positive and negative sides of the battery. This is accomplished by sending 250μA from the positive battery terminal through resistor R_2, then through the 1.2 volt AD589 bandgap reference, and finally back to the negative side of the battery via resistor R_{10}. This sets ground at 1.2 volts +3.18 volts (250μA × 12.7kΩ) = 4.4 volts below the positive battery terminal and 5.0 volts (250μA × 20kΩ) above the negative battery terminal. Bypass capacitors C_3 and C_5 keep both sides of the battery at a low ac impedance to ground. The AD589 bandgap reference establishes the 1.2 volt regulated reference voltage which together with resistor R_3 and trimpot R_4 set the zero dB reference current, I_{REF}.

The 3mV/dB scale factor of the dB output (pin 5 of the AD636) is changed to a more convenient 10mV output per dB input by the μA776 operational amplifier. Resistor R_{11} sets the amplifier's quiescent current at 100μA. Temperature compensation is provided via the series combination of resistors R_6 and R_7 which together produce an equivalent 2.1kΩ + 3325ppm/°C TC resistor (see the decibel input provision section).

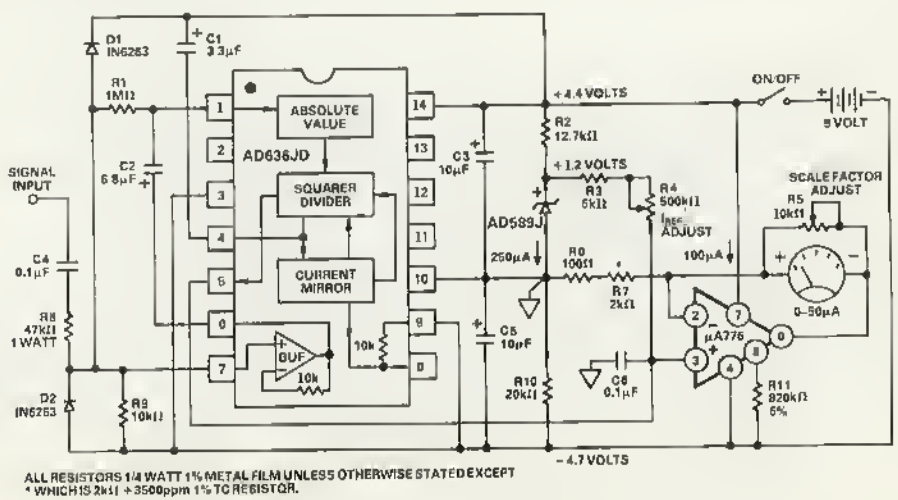


Figure 42. A Low Power, High Input Impedance dB Meter

Performance Data

0dB Referenee Range = 0dBm (770mV) to −20dBm
(77mV) rms
Input Range (at I_{REF} = 770mV) = 50dBm
Input Impedance = approximately $10^{10}\Omega$
V_{SUPPLY} Operating Range +5V dc to +20V dc
I_{QUIES} = 1.8mA typical

Accuracy with 1kHz sinewave and 9 volt dc supply:
0dB to −40dBm ±0.1dBm
0dBm to −50dBm ±0.15dBm
+10dBm to −50dBm ±0.5dBm

Frequency Response ±3dBm:
Input
0dBm − 5Hz to 380kHz
−10dBm = 5Hz to 370kHz
−20dBm = 5Hz to 240kHz
−30dBm = 5Hz to 100kHz
−40dBm = 5Hz to 45kHz
−50dBm = 5Hz to 17kHz

Battery Life

Using a standard 250mA/hour 9 volt transistor radio battery, normal battery life with the meter left on will be between 100 and 150 hours. A ten-fold increase in battery life can be achieved using a 2500mA/hour mercury power pack battery which should operate the circuit continuously for about two months. If a 9 volt nickel cadmium rechargeable battery such as the Eveready N88 is used, it can be kept charged by solar cells thus allowing maintenance-free operation. Requiring only about 1.8mA quiescent current, this meter lends itself well to many remote-site applications where changing batteries is inconvenient and expensive.

Calibration

1. First calibrate the zero dB referenee level by applying a 1kHz sinewave from an audio oscillator at the desired zero dB amplitude. This may be anywhere from zero dBm (770mV rms – 2.2 volts p-p) to −20dBm (77mV rms 220mV p-p). Adjust the I_{REF} cal trimmer for a zero indication on the analog meter.
2. The final step is to calibrate the meter scale factor or gain. Apply an input signal −40dB below the set zero dB reference and adjust the scale factor calibration trimmer for a 40μA reading on the analog meter.

Some final comments:

This meter is protected for input voltages up to 200 volts dc and has an input impedance of 10,000MΩ. Therefore, it is clearly superior to the circuits of Figures 34 and 35 for most all portable applications where the device may be exposed to all types of input signals and where very low power consumption is important.

Note: For the best possible resolution, the largest practical size analog meter movement should be chosen for use with this circuit.

The temperature compensation resistors for these circuits may be purchased from: *Tel Labs Inc*, 154 Harvey Road, P.O. Box 375, Londonderry, NH 03053, Part #Q332A 2kΩ 1% +3500ppm/°C or from *Precision Resistor Company*, 109 U.S. Highway 22, Hillside, NJ 07205, Part #PTI46 2kΩ 1% +3500ppm/°C.

A MODEM LINE MONITOR

This is a telephone line dB meter and line voltage sensor for the accurate monitoring and adjustment of telephone signal levels. The 600Ω line terminator doubles as a voltage sensor to detect dc voltage on the line. When switched on, the line terminator also keeps ringing voltage (90 volts @ 20Hz) off the line being measured by making the phone line appear busy to the telephone switching equipment. The user may self-check the meter calibration by pressing the calibrate switch on the front panel.

The input signal is ac coupled by C1 and runs through R_1 to pin 1 of the AD536A. Diodes D_1 and D_2 along with resistor R_1 protect the input of the AD536A from voltage spikes with capacitor C_2 and resistor R_1 forming a low pass filter.

The dB output from pin 5 of the AD536A runs directly to the input of the buffer amplifier. Zero adjust trimmer R_5 and resistor R_4 set the zero dB point on the analog meter by adjusting the amount of offset current from the AD580 voltage reference. Resistors R_9 and R_{10} form a voltage divider that "FLOATS" the AD536A common above ground, allowing single supply operation.

Capacitor C_4 is the averaging capacitor, while capacitors C_5 and C_6 are used for power supply bypassing. The dB output from the buffer amplifier (pin 6 AD536A) runs through meter calibration trimmer R_7 and resistor R_6 to a 50-0-50μA analog meter. Resistor R_8 provides a return path to ground.

To calibrate, first press the calibration switch and adjust R_5 to center the meter at zero with the chosen zero dB level applied. Decrease the input signal 30dB and adjust R_7 for −30dB.

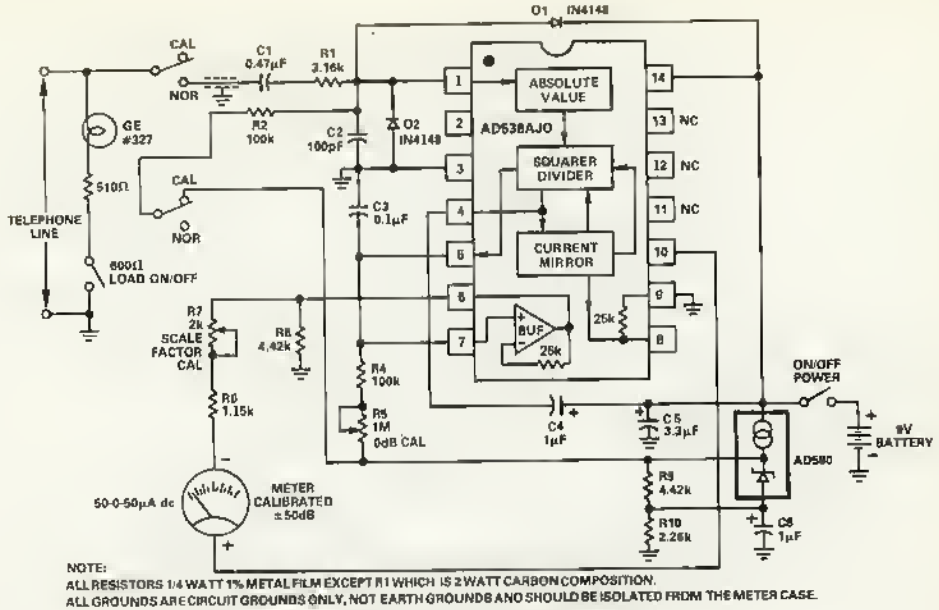


Figure 43. A Modem Line Monitor – A Telephone Line dB Meter

DATA ACQUISITION

A PROGRAMMABLE GAIN RMS MEASUREMENT SYSTEM

Introduction

The rms measurement of complex waveforms of varying magnitude normally requires a high quality, compensated input attenuator. In contrast, the programmable gain rms preamplifier circuit of Figure 44 features an AD544 bifet operational amplifier as an inverting input buffer with four remotely switchable gain ranges: 200mV, 2 volts, 20 volts, and 200 volts full scale. Switching gain resistors in the buffers feedback loop allows the use of a low voltage CMOS multiplexer to remotely control the gain of (potentially) high voltage input signals. The preamplifier's input is well protected on all ranges for input voltages up to 500 volts peak.

Circuit Description

The input signal is connected to input jack J_1 with resistor R_1 and diodes D_1 and D_2 forming the amplifier's input circuit protection. The diodes will conduct whenever the voltage at pin 2 of the AD544 exceeds either of the power supply voltages. Capacitor C_1 prevents high frequency roll-off, which would occur due to the R/C time constant of the 1MΩ input resistor and the stray capacitance at the AD544's summing junction. The AD7503 CMOS multiplexer switches the appropriate feedback resistor for each gain connecting the resistor between the operational amplifier output, pin 6, and its summing junction, pin 2.

Capacitors C_4 through C_7 are compensation capacitors which are adjusted for flat response at each gain setting. A_0, A_1, and A_2 are three address lines which select the desired input range of the preamplifier. R_4, R_6, R_{10}, and R_{12} are the gain calibration controls for each selected gain. The output of the AD544 operational amplifier is converted to its rms equivalent voltage by the AD536A rms-dc converter.

Performance Data:

Input Ranges: 200mV, 2 volts, 20 volts, 200 volts rms

	–3dB Bandwidth
200mV	≥4kHz*
2V	600kHz
20V	1.5MHz
200V	600kHz

Noise referred to amplifier input: 360µV rms on 2 volt range, 75dB signal to noise ratio. RMS converter settling time: 397ms to within 1% of change in

*Bandwidth will vary with the degree of stray capacitance at pin 9 of the AD7503.

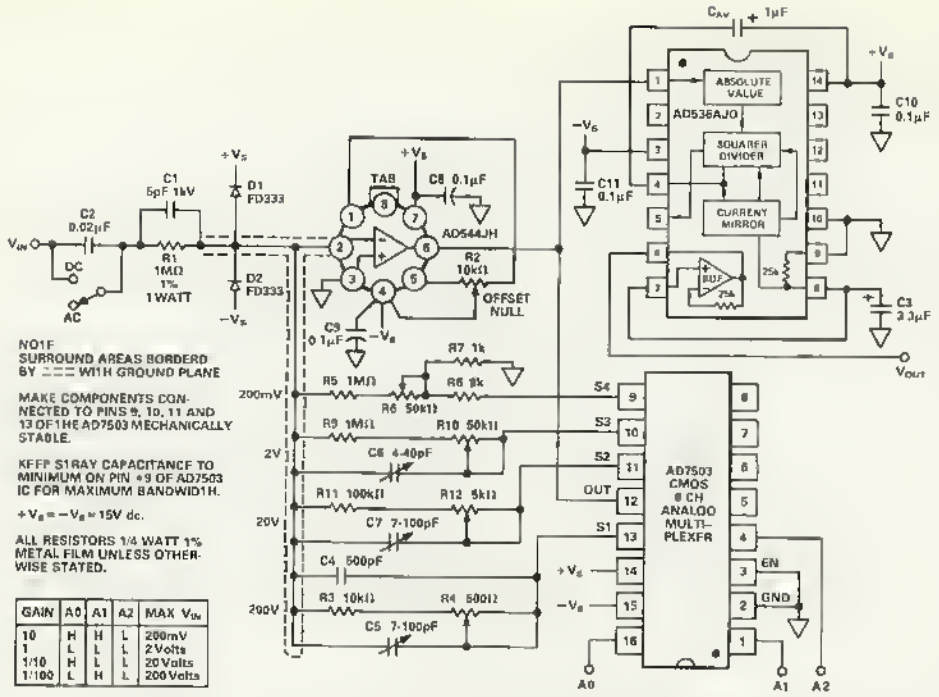


Figure 44. A Programmable Gain rms Measurement System

rms level of input. Power requirements: +5 volts dc @ 14mA ±15 volts dc @ 3mA.

Precautions

For maximum bandwidth and minimum input currents, capacitance at the summing junction (pin 2) of the AD544 must be kept to a minimum, and all points in the circuit connected to it should be Teflon insulated, or they should have a grounded guard ring surrounding them. The guard ring insures that leakage currents from the power supply pins or elsewhere are returned to ground and not to the summing junction.

As a safety precaution, the input jack and the wiring associated with it should be well insulated since potentially lethal voltages (200 volts rms) may be present.

Calibration

Address lines A_0, A_1, and A_2 should be set for each gain. The calibration trim potentiometers R_4, R_6, R_{10}, and R_{12} should be individually adjusted for the correct gain on each range.

The compensation capacitors C_5, C_6, and C_7 should be adjusted for flat response on each range by using a variable frequency sinewave input signal and either an oscilloscope to monitor the AD544 output, pin 6, or by using a digital voltmeter on its dc scale connected to the output of the rms converter.

LOW LEVEL RMS MEASUREMENT USING AN RMS INSTRUMENTATION AMPLIFIER

Introduction

The detection of low level signals can be made much easier and with greater accuracy by taking the required measurement differentially with an instrumentation amplifier (IA) rather than making an "unbalanced" measurement, employing an operational amplifier in one of the standard inverting or noninverting modes. To illustrate, an unbalanced input preamplifier such as that shown conceptually in Figure 45 can be severely compromised in terms of input noise discrimination from several standpoints. Unless the input voltage V_{IN} is a com-

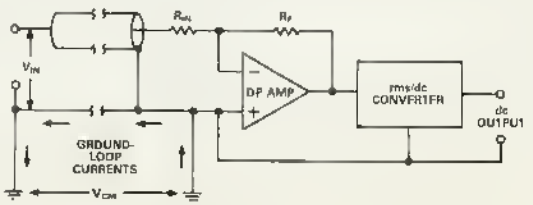


Figure 45. Noise in an Unbalanced System

pletely floating source, it will be difficult to cleanly amplify the signal because of the common mode voltage, V_{CM}.

In this system, both signal and ground loop currents flow in the shield line with the ground loop currents adding to the noise of the system. This added noise can make a low level measurement useless. In contrast to the operational amplifier, an instrumentation amplifier is a "gain block" which measures the *difference* between the voltages at its two inputs. This differential or balanced measurement method gives instrumentation amplifiers some distinct advantages, making them superior to standard operational amplifiers in many low level applications.

In the balanced measurement system of Figure 46, the shield line does not carry the input signal currents; it functions only as a shield. If there are any ground loop currents present, they simply are returned to common without adding to the noise of the system. Any noise that is picked up by the input lines will be "common mode" and cancelled out by the instrumentation amplifier. ($V_{OUT} = ((+V_{IN}) - (-V_{IN})) \times GAIN$).

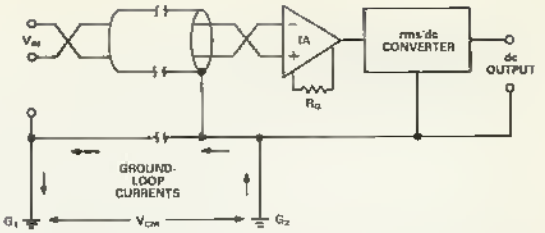


Figure 46. Noise in a Balanced System

Circuit Description

The rms-converter instrumentation amplifier scheme shown in Figure 47 uses a dual FET operational amplifier, an AD644, as a differential preamplifier.

This, in conjunction with the AD536A rms-dc converter, forms a high quality system for low level rms measurement. The preamplifier section of this system offers superior overall performance featuring: excellent common mode rejection of up to 90dB @ 1kHz, very low input bias current (typically 10pA), and a signal to noise ratio of −94dB.

The circuit of Figure 47 gives practical component values for two different system gains, 10 and 100 respectively. To select resistor values for other desired gains, use the formula:

$$\text{Gain} = 1 + \frac{R_3}{R_4} \text{ for: } R_1 = R_5 \text{ and}$$

$$R_3 = R_6 + R_7 + R_8$$

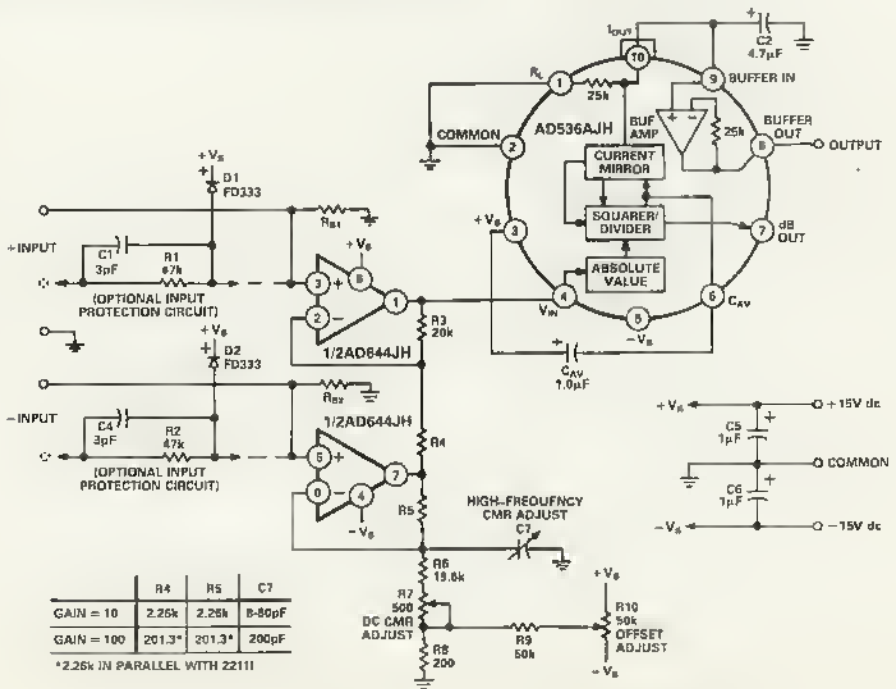


Figure 47. An rms Converter with an Instrumentation Amplifier Preamp

This circuit features a very high input impedance due to the FET operational amplifier input. However, there must be a return path to the ground potential of the converter portion, which is to say the preamplifier section cannot operate with totally floating sources, such as transformers or thermocouples. For such instances, two high value bias resistors can be added, RB_1 and RB_2, with a value of several megohms.

LOW FREQUENCY RMS MEASUREMENT

Introduction

As described in the previous sections, reducing the input frequency requires lengthening the averaging (and filtering) time contants to maintain the same levels of dc error and ripple. Consequently, successively larger values of C_{AV} are required as the input frequency is reduced. With the very large values of averaging capacitor necessary at frequencies below 10Hz, the physical size of the C_{AV} can occupy excessive board space and prohibit the use of the high quality, low leakage types that are the most useful at these frequencies.

Although the rms converter output filter section or sections can easily have their series resistance increased to give a longer averaging time constant (such as increasing Rx in Figure 24), the AD536A and AD636 averaging sections are not so flexible. Their fixed 25kΩ internal averaging resistors cannot be increased (see Figure 32). In these converters, averaging is carried out within the current mirror. The current, I_4, is averaged by C_{AV} and then ratioed (2×) to the output, via the current mirror, to the I_{OUT} terminal.

Fortunately, with the AD637 rms converter, averaging takes place within a filter stage which is externally accessible, shown in Figure 16. By reducing C_{AV} to 100pF (just enough capacitance to maintain stability), the filter stage becomes an output buffer, allowing external averaging. With this connection, very large resistance values (and therefore much smaller averaging capacitors) may be used. The circuits of Figures 48 and 49 use this concept to produce averaging times of several seconds, yet requiring relatively small averaging capacitor values.

A Low Frequency RMS-DC Converter Circuit

Figure 48 is a low frequency rms to dc converter circuit optimized to give less than 0.1% averaging error for frequencies down to 1Hz. With this circuit, averaging is carried out *between* the rms output terminal, pin 9, and the input to the internal buffer amplifier, pin 1. The buffer amplifier successfully isolates the 25kΩ input impedance of the denominator input pin from the averaging section preventing that sec-

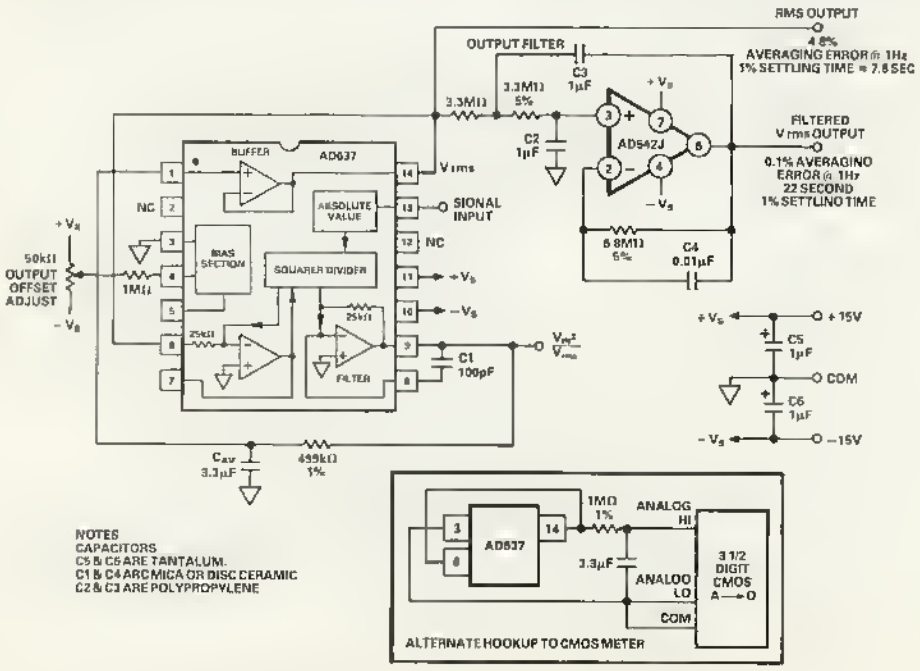


Figure 48. A Low Frequency rms to dc Converter Circuit

tion from being loaded down; it also provides the output buffering necessary to drive external circuitry. Rather than being directly connected to pin 9, the denominator input is now tied to pin 14, receiving its feedback via the output of the buffer amplifier. The rms output may be taken from either the buffer output pin for a 4.8% averaging error output (thus giving a high error output with minimum settling time) or from the output of the external output filter whose filtering reduces the averaging error to less than 0.1% (at the expense of increased settling time).

A useful by-product of utilizing the external component averaging scheme just mentioned is that by making the AD637 filter section a simple voltage follower, a new output function, V_{IN}^2/V_{rms}, now becomes available.

An Ultra-Low Frequency RMS-DC Converter Circuit

The circuit of Figure 49 operates in a similar manner to that of Figure 48 except that it uses two very low input bias current amplifiers which permit even larger values of averaging resistance, in this case 10MΩ, to be used.

This circuit has been optimized to exhibit less than 0.1% averaging error for input signals as low as 0.1Hz. As with the previous circuit, the V_{IN}^2/V_{rms} function appears at pin 9 of the AD637.

Note:

The two low frequency rms measurement circuits described in this section may overload on transient noise spikes, such as those at power line frequencies. This occurs because the filter stage averaging capacitor (normally called C_{AV} but in these circuits, it has been renamed C_1) has been drastically reduced. This allows the output at pin 9 of the AD637 to respond to the *square* of the input signal rather than to the *average of the square* of the input. For example, if a 1 volt peak transient appears at the input of the rms converter while the circuit is measuring a 10mV rms input signal, the output at pin 9 should theoretically equal:

$$V_{OUT} = \frac{V_{IN}^2}{V_{rms}} = \frac{(1\text{ volt})^2}{0.01\text{ volts}}$$

$$= 100\text{ volts!}$$

Obviously, the output will saturate long before it approaches 100 volts, creating a large error which *may not be noticed* as such at the filtered V_{rms} output point due to the extensive RC filtering between this point and pin 9 of the rms converter. Therefore, for general purpose applications where the V_{IN}^2/V_{rms} function is not needed or for applications where high crest factor-low frequency signals are to be measured, it is recommended that capacitor C_1 be increased to 3.3μF. This capacitor, in conjunction with the internal 25kΩ filtering resistor, will form a low pass filter with a 2Hz corner frequency. This will attenuate higher frequency signals, i.e., transients, by the ratio of the transient frequency to that of 2Hz. This means that in the case of 60Hz transients, they will be re-

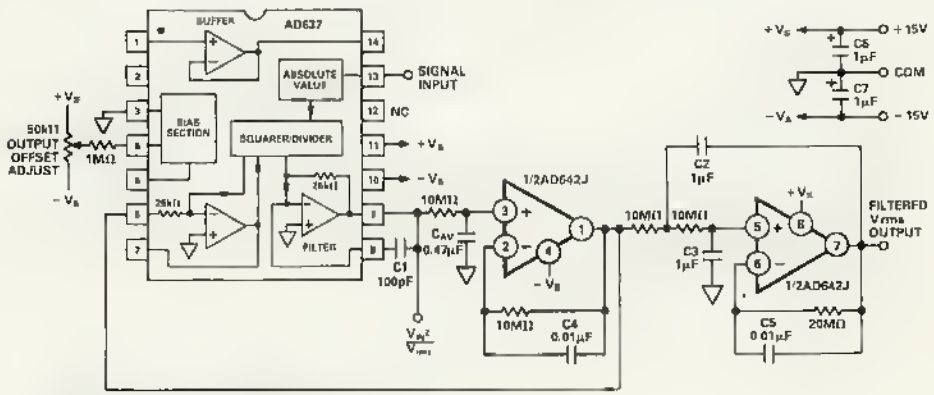


Figure 49. An Ultra-Low Frequency rms to dc Converter Circuit

duced by 60Hz/2Hz or 30 times. Therefore, practically speaking, there will be effective transient protection.

In addition, larger or smaller values of C_1 may be used as required by the specific application. If a low pass filter is used ahead of the AD637, out of band signals are less likely to cause an overload; this allows smaller values of C_1 to be used in these circuits.

Since increasing C_1 causes the increased averaging of higher frequency signals, the V_{IN}^2/V_{rms} function will be linearly converted to the average of V_{IN}^2/V_{rms} as the input frequency goes up. This prevents the instanteous square of the input signal from appearing at pin 9 of the AD637.

APPENDIX A

TESTING THE CRITICAL PARAMETER OF RMS CONVERTERS

INTRODUCTION

RMS converters share many basic characteristics with precision rectifier circuits; therefore, most of their testing is similar in nature. However, there are two basic parameters of rms converters that must be evaluated differently; one is error versus crest factor which is usually not tested at all in precision rectifier circuits. The other parameter is ac accuracy or bandwidth, which may be specified for 1% additional error or for a ±3dB change.

Adequate performance in both of these parameters is important to insure that the rms converter can properly compute the rms value of an incoming pulse or other waveform containing significant harmonic content. This also insures that both the rise time and slew rate of the converter are sufficiently fast to avoid rolling off the edges of incoming pulse trains.

The following sections in this appendix give detailed examples of the practical test setups and procedures necessary to properly evaluate the performance of an rms converter.

TESTING ACCURACY VERSUS CREST FACTOR

One of the critical parameters that defines an rms converter's performance is its accuracy as a function of the crest factor of its input waveform (see Section 1). Since average responding devices such as precision rectifiers have considerable errors when measuring nonsinewave input signals, this parameter applies only to *true* rms converters.

Figure 50 shows a test setup for measuring accuracy versus crest factor. A function generator or pulse generator is followed by an rms–AGC amplifier (see Figure 36) whose output is a constant rms voltage. This device greatly simplifies the task of maintaining a constant rms output while varying the function generator duty cycle to obtain the various crest factors needed to test the rms converter. Because of the different measuring methods of the two pieces of test equipment, the true rms meter monitors the *rms* level of the input waveform supplied to the rms converter while the oscilloscope connected to the same point gives a visual display of the *peak* amplitude of the waveform. The crest factor of the input waveform can then be found by dividing its peak value by its rms value.

$$\text{Crest Factor} = \frac{\text{Peak voltage (from oscilloscope)}}{\text{RMS voltage (from true rms meter)}}$$

The digital voltmeter monitors the output of the rms converter. The difference between the readings of the rms meter and the digital voltmeter will equal the error of the rms converter. The error in percent of reading is equal to this voltage divided by the true rms voltage times 100%.

$$\text{Error \% of Reading} = \frac{\text{Error voltage}}{\text{True rms voltage}} \times 100\%$$

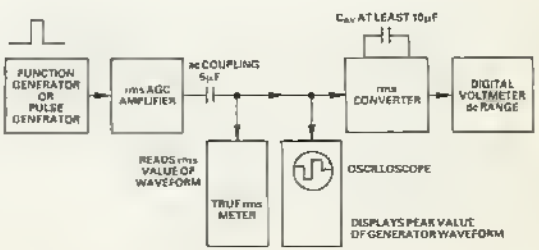


Figure 50. A Crest Factor Test Set-Up

Testing ac Accuracy (or Bandwidth vs. Input Level)

Two basic methods for testing the ac accuracy of rms converters are commonly used. The first method maintains accuracy by using a true rms meter to monitor the level of a sinewave oscillator which feeds the input of the rms converter under test (Figure 51). A digital voltmeter measures the dc output of the rms converter. The voltage reading of the true rms meter is then compared to that of the digital voltmeter. Accuracy is specified as a percent of reading error. AC coupling of the sinewave oscillator output is used to prevent any dc offset that may be present at the output from being measured by the rms converter.

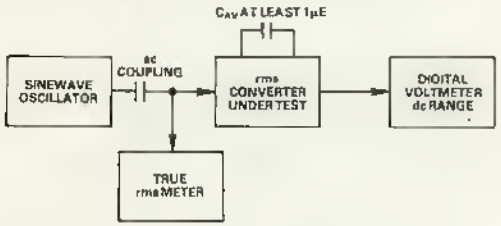


Figure 51. Testing ac Accuracy

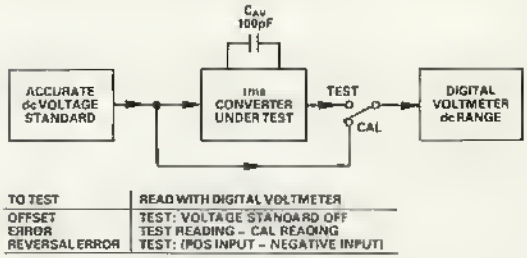
A second and more accurate method for measuring ac accuracy involves the use of a precision ac voltage standard to replace the sinewave oscillator and true rms meter of the previous method (see Figure 52). This has the advantage of a much improved ease of operation since the desired test voltage may simply be dialed in (the first method required a careful adjustment of the oscillator output level for each change in test voltage). However, an unfortunate disadvantage of this method is the relatively high cost of a precision ac voltage standard.

Figure 52. Testing ac Accuracy – Alternate Method

TESTING CONVERSION ACCURACY

DC Accuracy

In the scheme of Figure 53, a cal/test switch is set to the calibrate position, and a dc reference is adjusted for the desired dc input voltage and polarity. The reading on the digital voltmeter then compares the difference between the test and calibration positions. The dc error is specified as a maximum percent of reading plus or minus the input offset voltage of the device under test (which is the zero input reading). The dc reversal error is the maximum difference between the positive and negative input readings and is specified as a percent of reading.



TO TEST	READ WITH DIGITAL VOLTMETER
OFFSET ERROR	TEST: VOLTAGE STANDARD OFF TEST READING – CAL READING
REVERSAL ERROR	TEST: (POS INPUT – NEGATIVE INPUT)

Figure 53. Testing dc Accuracy

Linearity

Figure 54 shows a setup for testing the linearity of rms converters over their full range of input amplitudes. For dc linearity, an accurate variable dc reference is used as the input source. For measuring ac linearity, a sinewave generator and a precision attenuator replace the dc standard. The precision attenuator is used to obtain very close ratios of input voltage while retaining their original wave shape. A unity gain output buffer should follow the attenuator to prevent the rms converter input circuit from loading it down.

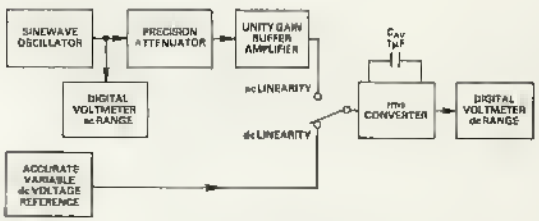


Figure 54. Testing Linearity

USE OF CROSSPLOTS TO SPEED TESTING OF RMS CONVERTERS

Introduction

The use of an X-Y or crossplot display method using an oscilloscope is a very useful tool for evaluating the performance of precision rectifiers and the offset and linearity of rms converters. The X-Y pattern gives, at a glance, a visual display of input offset, output offset, scale factor, and linearity of a rectifier circuit. Parasitic oscillations and other elusive problems frequently undetected by automatic test equipment are very noticeable using this method.

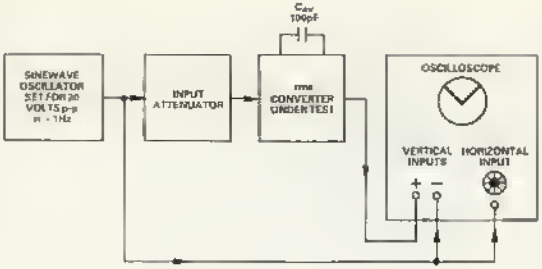


Figure 55. A Crossplot Test System

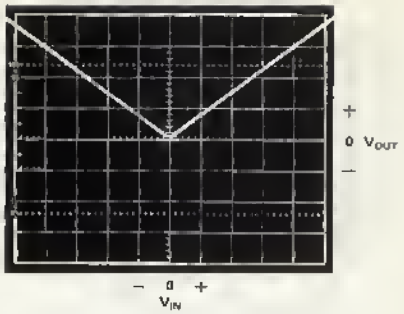


Figure 56. An Ideal Crossplot Pattern

Setting Up the Crossplot Test System

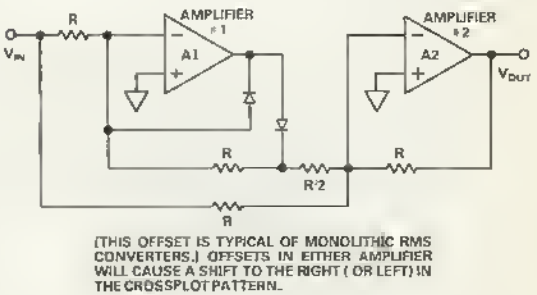
A crossplot test system can be easily set up using ordinary laboratory test equipment. This equipment should consist of a sine-wave oscillator or function generator, an accurate input attenuator (or an oscillator incorporating a precision attenuator), and an oscilloscope with a differential input preamplifier. If possible, the oscilloscope should use a Tektronix 7A22 or similar type variable bandwidth preamplifier to filter any stray noise pickup at low input voltages.

Figure 55 illustrates the correct method for interconnecting the test equipment for a crossplot test setup. The sine-wave oscillator output connects to the rms converter's input as well as the oscilloscope's vertical and horizontal input jacks. The output from the rms converter connects to the oscilloscope's positive vertical input jack. With the negative or inverting vertical input switched off or disconnected, this setup will measure the slope of the rms converter as well as its input and output offset voltages.

With the negative vertical input switched on, the vertical amplifier of the oscilloscope acts as a subtractor amplifier. The oscilloscope will then display the rms converter's linearity. For this test, the oscilloscope preamplifier is considered to be an "ideal" subtractor amplifier.

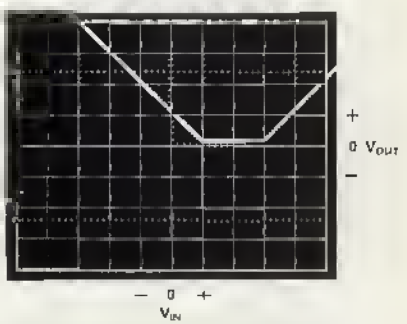
Evaluation of Crossplot Patterns

The crossplot pattern of Figure 56 displays an "ideal" slope pattern with no offsets. The sine-wave input voltage is displayed on the oscilloscope's horizontal axis. For a 20 volt peak-to-peak input signal, the horizontal amplifier of the oscilloscope should normally be set for 2 volts per horizontal division with the zero input level occurring at the zero axis crossing. The rms converter's output is displayed on the oscilloscope's vertical axis, and since it is of one polarity (in this case positive), it will lie entirely on one side of the zero axis. The vertical axis amplitude will rise and fall with the amplitude of the sine-wave input voltage. For these tests, the rms converter's averaging capacitor should be disconnected and replaced with a minimum sized unit, (typically



(THIS OFFSET IS TYPICAL OF MONOLITHIC RMS CONVERTERS.) OFFSETS IN EITHER AMPLIFIER WILL CAUSE A SHIFT TO THE RIGHT (OR LEFT) IN THE CROSSPLOT PATTERN.

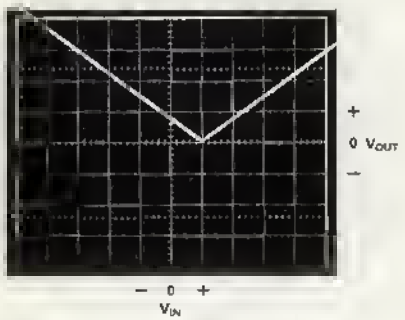
Figure 57. Two Amplifiers are Used in the Absolute Value Circuit



THIS OFFSET CREATES A FLAT SPOT OR "DEAD ZONE" IN THE INPUT TO OUTPUT TRANSFER CHARACTERISTICS. THE FLAT SPOT IS PRODUCED BECAUSE THE ABSOLUTE VALUE CIRCUIT WILL NOT ALLOW THE CONVERTER OUTPUT TO GO NEGATIVE. THE CENTER OF THE SHIFT MAY BE ON EITHER SIDE OF $0V_{IN}$ DEPENDING ON WHICH INPUT AMPLIFIER HAS THE OFFSET.

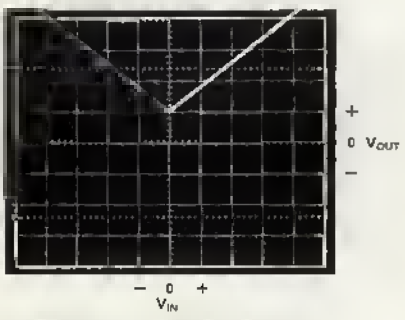
Figure 58. Input Offset in Absolute Value Circuit

100pF), otherwise, its output would simply be a straight horizontal line whose vertical amplitude would equal the rms equivalent voltage of the input signal.



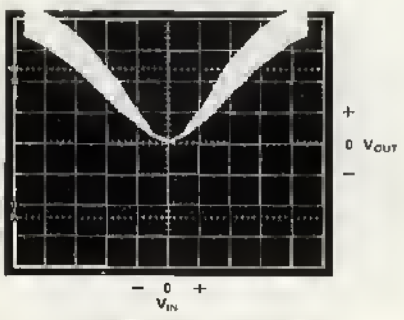
THE INTERSECTION POINT, OR BOTTOM TIP OF THE "V", MAY OCCUR ON EITHER SIDE OF $0V_{IN}$ DEPENDING ON WHICH AMPLIEIER IN THE ABSOLUTE VALUE CIRCUIT HAS THE OFFSET.

Figure 59. Input Offset in Absolute Value Circuit



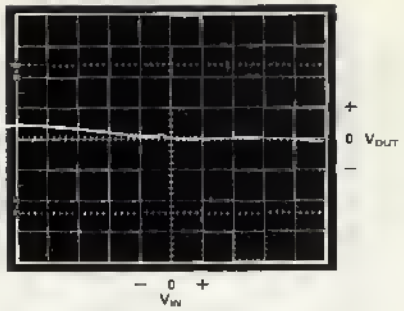
THE INTERSECTION POINT, THE BOTTOM TIP OF THE "V", MAY OCCUR TO EITHER SIDE OF $0V_{OUT}$ DEPENDING UPON THE POLARITY OF THE OFFSET.

Figure 60. Offset at Amplifier Output



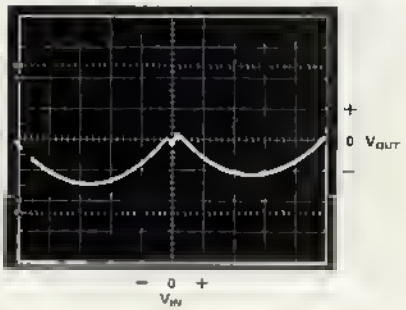
THIS WAVEFORM INDICATES DYNAMIC INSTABILITY PROBLEMS IN AN rms CONVERTER.

Figure 61. Oscillation/Instability



THIS PATTERN INDICATES AN rms CONVERTER HAS A LINEARITY CLOSE TO THAT OF AN "IDEAL UNIT. APPROXIMATELY 0.01% @ 5mV PER VERTICAL DIVISION

Figure 62. Good Linearity



THIS CROSSPLOT PATTERN IS BOWED AND UNSYMETRICAL. APPROXIMATELY 0.4% @ 50mV PER VERTICAL DIVISION.

Figure 63. Poor Linearity

AN RMS CROSSPLOT TESTER

This precision tester will measure the offsets and errors of rms converters and precision rectifiers. The unit requires ± 15 volt power supplies and an audio generator.

Circuit Description

From the input jack a 20 volt peak-to-peak signal generator voltage is divided down by an input attenuator which is used to select the desired input voltage range for the device under test. Amplifier A_1, an input buffer, drives the center of the symmetry potentiometer and the precision rectifier circuit; these would load down the input attenuator without buffering. Amplifier A_2, a precision half-wave rectifier, in conjunction with summing amplifier A_3, form a precision full-wave rectifier circuit. Amplifier A_3 has provision for either variable gain or fixed, preset gain.

With switch S_2 in the error mode, the output of the precision rectifier is compared to the output of the

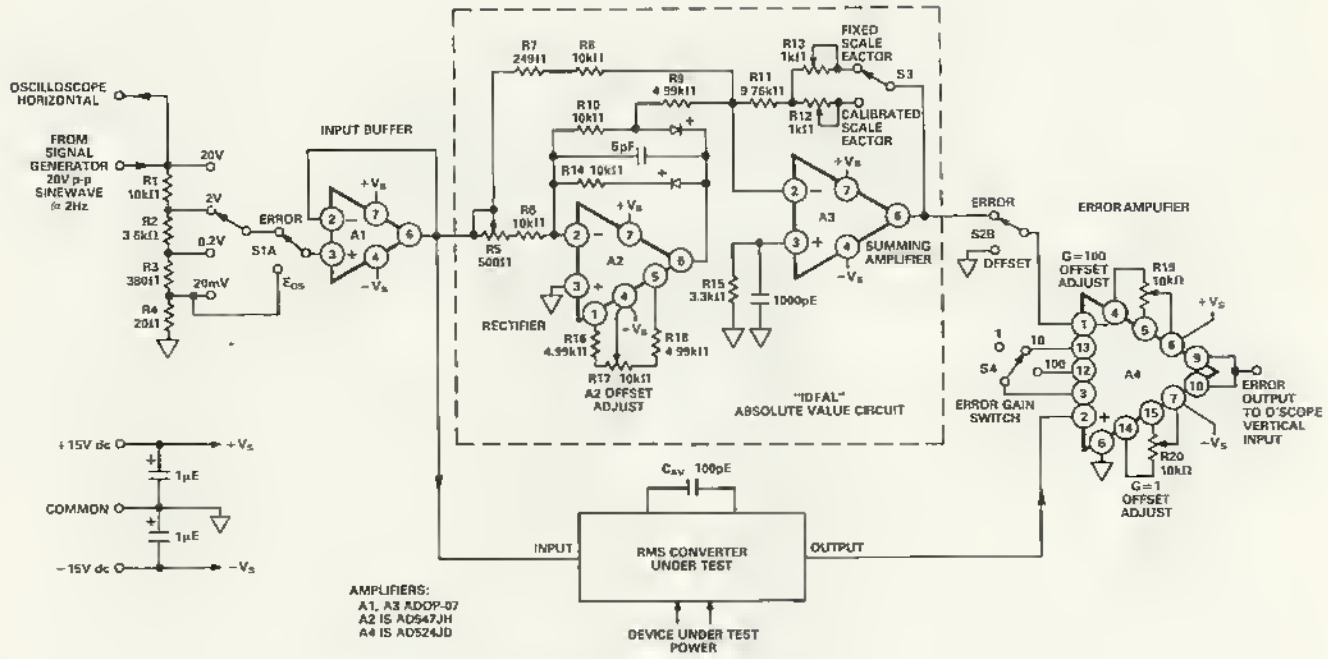


Figure 64. An rms Crossplot tester

device under test by error/amplifier A_4; this *difference* output is the error of the device under test. (The precision circuit is carefully calibrated and is assumed to be "perfect"). This amplifier operates at several selectable voltage gains, and, therefore, the error output of the test box will be the actual error the device under test times the gain of amplifier A_4. When S_2 is in the E_{OS} position *no* subtraction takes place, therefore, this position is used for checking the slope and offset of the rms converter under test (refer to the previous section).

The 100pF averaging capacitor C_{AV} is used for stability of the rms converter under test and does not average out the input waveform, thus the converters operate as precision rectifiers for testing purposes. Separate power supply jacks should be provided for testing the AD636 rms converter which operates at lower power supply voltages, typically +3V and −5 volts dc.

Calibration

Step 1. Using an oscilloscope with vertical and horizontal preamplifiers connected to their respective jacks on the rms crossplotter, adjust trim potentiometer R_{17} for a symmetrical "V" pattern with the input selector on the 20mV position and the input jack connected to an audio sine-wave generator adjusted for 20 volts peak to peak at ≈ 1Hz. The "V" should be centered and equal on both sides.

Step 2. With gain switch S_4 set for a gain of 1, adjust trim potentiometer R_{20} for zero output offset as shown in Figure 56.

Step 3. Repeat step 2, setting S_4 for a gain of 100. Adjust trim potentiometer R_{19}.

Step 4. With a dual polarity 10 volt dc reference connected to the generator input jack, alternate the polarity of the reference back and forth from plus to minus to adjust the symmetry trim potentiometer R5 for equal readings of + 10.000 volts dc from pin 6 of A_3 to ground as measured by a high input impedance digital voltmeter.

Step 5. Finally, adjust trim potentiometer R_{13} for the correct slope, i.e., scale factor as shown in Figure 56.

APPENDIX B

INPUT BUFFER AMPLIFIER REQUIREMENTS

THE NECESSITY OF AN INPUT BUFFER

The characteristic input impedance of the AD536A is approximately 7kΩ, the AD637 8kΩ, and that of the AD636 closely approximates 6.7kΩ.

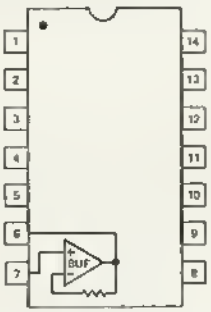


Figure 65.

Virtually all packaged rms to dc converters have an input resistance of less than 100k ohms. These impedance values are far too low for the rms converters to be used directly following high impedance inputs, such as input attenuators and must be driven by some type of buffering amplifier for these applications.

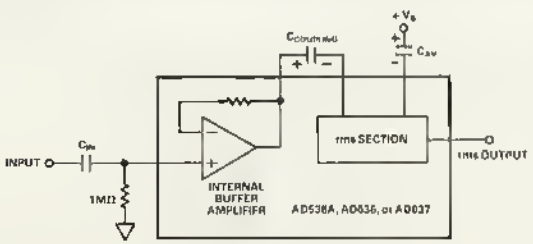


Figure 66. A Simple Input Buffer Connection Using the Internal Buffer Amplifier of an rms Converter

USING THE AD536/AD636 INTERNAL BUFFER AMPLIFIER AS AN INPUT BUFFER

With the circuit of Figure 66, the 1MΩ resistor provides a dc return for the signal path to ground. Without this resistor, the input bias current will charge up C_{IN} and saturate the buffer amplifier.

This simple input buffer scheme has several disadvantages. The 1MΩ input impedance is still too low a value for use following input attenuators (typically 10MΩ impedance). Also, the amplifier is prone to input overload at the higher frequencies (above 100kHz).

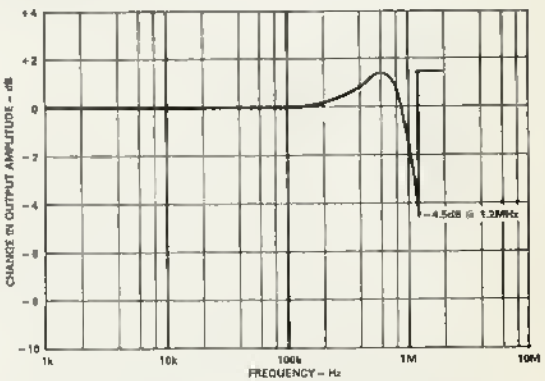


Figure 67. AD536A Internal Buffer Amplifier Relative Output Response vs. Frequency (1 Volt P/P Input Level – No Load Condition)

One simple improvement to this circuit is the addition of a series input resistor, R_{IN}, which in conjunction with the stray input capacitance of the operational amplifier forms a low pass filter. The input signal is then sufficiently attenuated at frequencies above 100kHz to prevent input overload. A further

improvement, the addition of a 47kΩ series resistor and two low leakage diodes provides a high degree of input protection from transients (via external sources) which could destroy the buffer (see Figure 68).

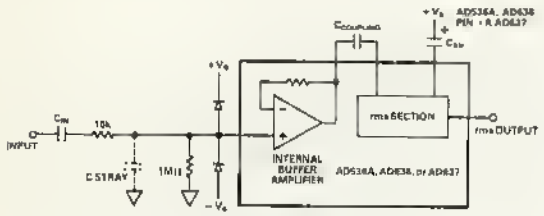


Figure 68. An Improved Input Buffer

BOOTSTRAPPING AN RMS CONVERTER'S INTERNAL BUFFER AMPLIFIER (FIGURE 69)

What is Bootstrapping?

A very effective method for dramatically raising input impedance is through the use of bootstrapping. This has the effect of multiplying the input impedance by the open loop gain of the amplifier.

With the buffer connection of Figure 68, the input resistor is returned to ground setting the effective input impedance approximately equal to the value of that resistor. The trick with bootstrapping is that since the buffer amplifier is operated as a unity gain voltage follower, its output voltage will equal the voltage of its input. Using the bootstrapping circuit of Figure 69, the input resistor, R_2, is now connected between the amplifier's input and output. Since (assuming an ideal amplifier) both sides of this resistor are at equal potential, the input impedance of the buffer amplifier is not effected (ideally) by the resistor and remains extremely high. With practical circuits, the amplifier does not have infinite open-loop gain and an error voltage will appear across R_2. This makes the effective input resistance of the circuit equal to the series protection resistor R_1 plus the product of input resistor R_2 multiplied by the open loop gain of the amplifier.

$$R_{IN} = R_1 + (R_2 \times A_{OL})$$

R_{IN} can be quite high ($\pm 10^9\Omega$) since the buffer amplifier (of the AD536A and AD636) typically has an open loop gain of 2,000 (at dc).

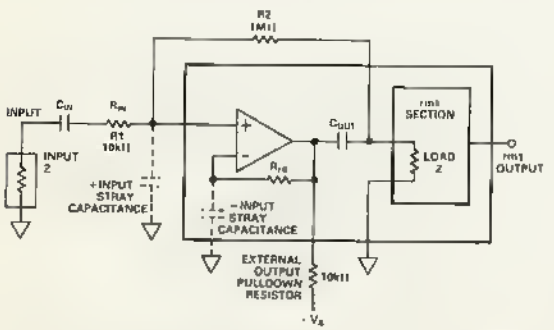


Figure 69. Using the Internal Buffer Amplifier as a Bootstrapped Input Buffer

Some Precautions

Bootstrapping does require a few precautions: Problems may arise due to stray capacitance at the inverting input of the amplifier. At high frequencies, the internal feedback resistor (R_{FB}) of the converter's buffer amplifier in conjunction with the stray capacitance at the inverting input form a voltage divider. (A second divider is formed via resistor R_1 and the stray capacitance at the noninverting input.) Depending on both the magnitude of the strays and the input signal frequency, the circuit's stray capacitances may cause the amplifier to operate *with gain* and cause instability. Capacitor C_{OUT} ac couples the output; connecting the input resistor to the input *after* this coupling capacitor prevents dc latchup problems.

The dc return path for the buffer's input current is via the load impedance of the rms section of the rms converter following the buffer. The bias current travels through resistor R_2 and then to ground via the relatively low input resistance of the rms section.

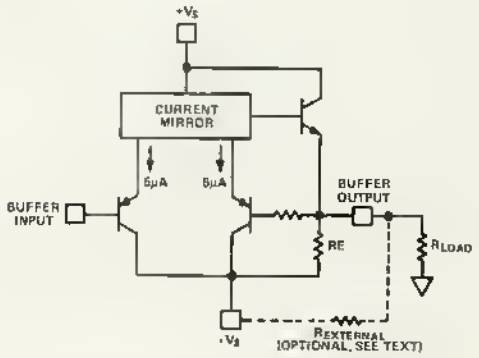


Figure 70. AD536A, AD636, AD637 Internal Buffer Amplifier Simplified Schematic

BUFFER AMPLIFIER OUTPUT STAGE CONSIDERATIONS

The AD536A/AD636/AD637 buffer amplifier does not employ the usual Class AB complementary output stage but uses a Class A emitter follower output instead (see Figure 70). This allows the output voltage to swing fully to ground during single supply operation as an output buffer.

However, when using this amplifier as an *input* buffer, steps must be taken to insure an adequate negative output voltage swing. For negative outputs, current must travel through the buffer's internal emitter resistor, R_E. The maximum current that the output stage can obtain from the negative supply is therefore limited by the value of R_E. This in turn limits the maximum negative output voltage swing the buffer may provide for a given value of load resistance (i.e., resistor R_E and the load resistance R_{LOAD} form a voltage divider limiting the maximum negative voltage output of the buffer).

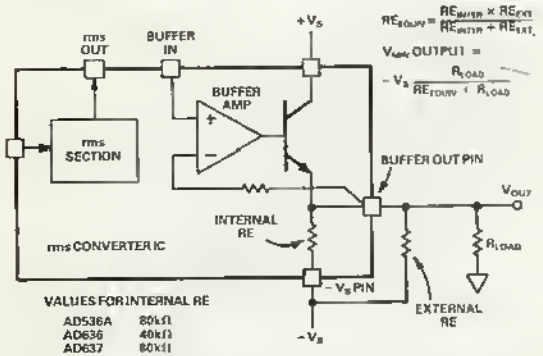


Figure 71. The Effect of $R_{Eequivalent}$ and R_L on the Maximum Output Swing of the AD536A, AD636 and AD637 Internal Buffer Amplifier

An obvious way to increase negative output voltage swing is to add an external resistor between the amplifier output (a transistor's emitter) and $-V_S$. Unfortunately, the addition of this resistor ($R_{E\ external}$) will increase the buffer amplifier's quiescent current. Therefore, *proper operation of the buffer will be a compromise between maximum output voltage swing and amplifier quiescent current.*

A 30% overrange below the minimum desired output voltage swing is a good rule of thumb. The effective R_E between the transistor's emitter and $-V_S$ is the parallel combination of the two resistors R_E and $R_{E\,external}$.

That is: $$R_{E\,effective} = \frac{R_E \times R_{E\,external}}{R_E + R_{E\,external}}$$

The equation for maximum output swing is:

$$V_{MAX} = V_S \times \frac{R_{LOAD}}{\frac{R_E \times R_{E\,external}}{R_E + R_{E\,external}} + R_{LOAD}}$$

Combining the two equations:

$$R_{E\,external} = \frac{R_E R_L (V_S - V_{MAX})}{R_E V_{MAX} + R_L (V_S - V_{MAX})}$$

This formula may be used for calculating the value of the external emitter resistor required.

An alternative method for determining $R_{E\ external}$ is to use Figure 72. This should be done after calculating the ratio of $V_{MAX}/V_{-SUPPLY}$ for the particular application. The value of $R_{E\ external}$ is the point on the graph where $V_{MAX}/V_{-SUPPLY}$ intersects the value of R_L.

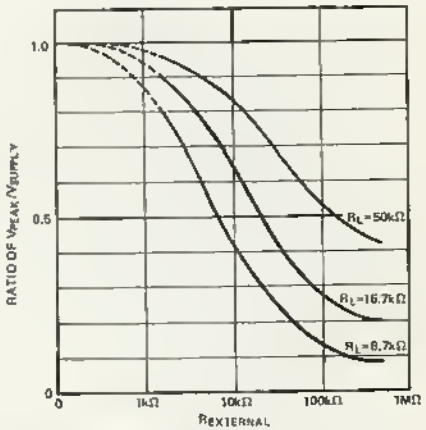


Figure 72. AD536A, AD636, AD637 Internal Buffer Amplifier – Ratio of Peak Negative Output Swing to $-V_S$ vs. $R_{Eexternal}$ for Several Load Resistances

Note: The AD637 buffer amplifier is too slow to drive its rms section over its entire bandwidth. However, it is useful in applications where 100kHz bandwidth is adequate and the greater accuracy of the AD637 (as compared to the AD536A) is important. The following section of this guide explains the special performance requirements demanded of an input buffer used with a wide bandwidth rms converter such as the AD637.

AD637 INPUT BUFFER AMPLIFIER REQUIREMENTS

Bandwidth and Slew Rate Limitations

The AD637 is a very high speed rms converter, providing up to 5MHz bandwidths with 1 volt rms input signals. However, with this much bandwidth available, serious consideration must be given to the choice of the input buffer amplifier if the full high frequency performance of the rms converter is to be realized. Obviously, an input buffer such as that shown in Figure 73 must have a ±3dB bandwidth several times greater than that of the rms converter to avoid introducing additional errors. This fact is usually considered when an input buffer is selected,

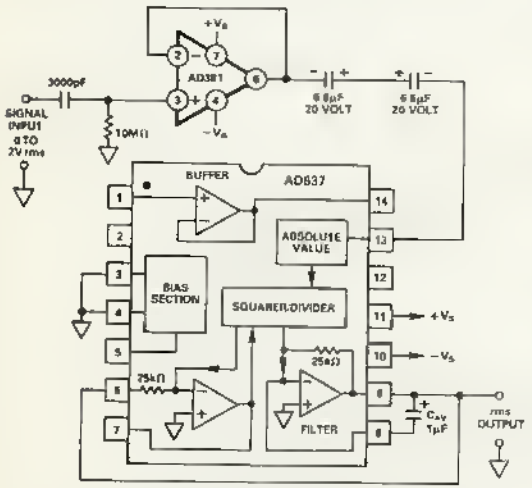


Figure 73. AD637 rms Converter with External 4MHz. High Impedance Input Amplifier

and several commonly available amplifiers have adequate bandwidths to meet this requirement. What is most commonly over looked is the fact that the amplifier's *slew rate* requirements may be considerable! As an example:

For an input buffer amplifier driving a 5MHz rms converter with a *sinewave* of 1.4 volts peak amplitude (1 volt rms), the maximum slew rate required can be found:

$V = A_m \sin\omega T$

WHERE: V = Instantaneous Voltage
A_m = Peak Amplitude of the waveform
ω = 2π Times the frequency of the input waveform
T = Period of the input waveform

Since. . . Slew Rate $= \frac{\Delta V}{\Delta T}$ Then:

$$\text{Slew Rate} = \frac{dV}{dT} = A_m\,\omega\cos\omega T$$

The maximum slew rate of a sine wave is at the origin and at this point $\cos\omega T = 1$
Therefore:

Maximum Slew Rate $= \frac{\Delta V}{\Delta T} = A_m\,\omega =$
$V_{peak}\,(2\pi F)$ where F = input frequency in Hz

This means that the maximum slew rate required from an amplifier in volts per microsecond will equal V_{peak} times 6.28 times the input frequency in megaHertz. For the example given above:

Maximum Slew Rate required will equal 1.4 volts times 6.28 times 5 megaHertz or 44 volts per microsecond.
For a three volt rms input level, the maximum slew rate required would be 133 volts per microsecond.

Figure 74 displays the full range of minimum slew rate required for a sine-wave input of up to 7 volts rms applied. This may be used for roughly calculating input buffer requirements.

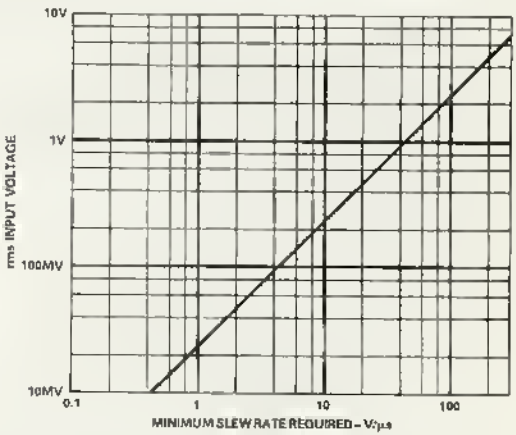


Figure 74. Minimum Slew Rate Required from an Input Buffer Amplifier Driving a 5MHz rms Converter in Volts/Microsecond

Figure 75 shows the actual −3dB bandwidth of the circuit of Figure 73. Note that up to approximately 400mV this circuit is bandwidth limited by the bandwidth versus input characteristics of the rms converter; above this level, however, the slew rate

limitations of the 30V/μs input amplifier limit the overall bandwidth of the system. Peak bandwidth for this circuit occurs where converter bandwidth is high and where the input amplifier is still slewing adequately.

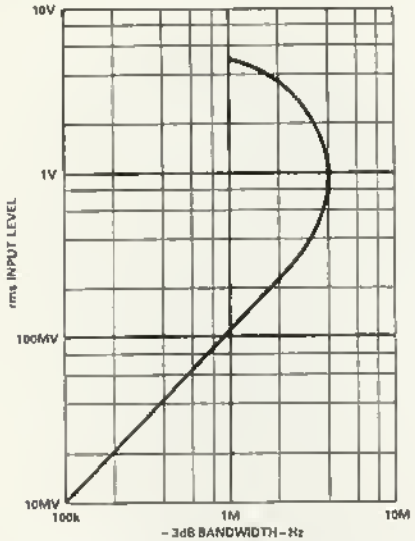


Figure 75. AD637 with AD381 Input Buffer Amplifier –3dB Bandwidth vs. Input Level

A final consideration regarding input amplifier slewing rate: the amplifier must slew symetrically, that is, go as fast in the negative direction as in the positive, otherwise the slew rate in the slower direction will limit overall bandwidth. It is especially important to avoid using some common bifet amplifiers whose slew rates vary as much as 2 to 1 thus making them unsuitable for this high speed application. The AD381 operational amplifier is a good example of the type of amplifier which should be used ahead of an rms converter as an input buffer; it has symmetrical slew rate characteristics, a high slew rate, adequate bandwidth, good dc specifications, and it is a low noise device.

Buffer Amplifier Frequency Compensation

Input buffer amplifiers that are externally compensated should be carefully "tweeked" for the best possible square-wave response since overshoot, ringing, and other instability problems in op amps will cause peaks in the bandwidth characteristics of these amplifiers.

APPENDIX C

COMPUTER PROGRAMS FOR COMPUTING COMPUTATIONAL ERRORS, OUTPUT RIPPLE, AND 1% SETTLING TIME FOR RMS CONVERTERS

Introduction

Rather than use filter charts or formulas, many people may prefer to use a computer program to perform calculations. The following programs have been written for the Apple II Computer. The first calculates values of dc error, ripple, and averaging error for each of the three basic connections (i.e., C_{AV} only, one pole post filter, two pole sallen-key filter).

For the one pole filter case, output values using C_2 equal to 2.2 times C_{AV} and 3.3 times C_{AV} will be automatically printed out when the one pole filter case is selected. For the two pole filter, capacitors C_2 and C_3 are both set equal to 2.2 times C_{AV}.

The second computer program calculates the total settling time for each connection using the values of C_{AV}, and/or C_2 and C_3 selected.

PROGRAM #1

RMS CONVERTER RIPPLE/ERROR PROGRAM

```
10   REM  FROM ANALOG DEVICES SEMICONDUCTOR
20   REM  WRITTEN BY CHARLES KITCHIN AND ANDREW WHEELER
30   REM MARCH 22, '83
40   REM PROGRAM TO COMPUTE %D.C. ERROR AND % RIPPLE IN RMS CONVERTERS
50   DIM E(20),F(20),R(20),R2(20),R3(20),AV(20),A2(20)
60   HOME : VTAB 4: PRINT "RMS CONVERTER ERROR/RIPPLE PROGRAM"
70   PRINT "*********************************": PRINT
80   INPUT "ENTER CAVG VALUE IN UF : ";C1
90   PRINT "*********************************"
100 M = .025:T = (M * C1):M1 = .0245:PL = 0
110 C(2) = 2.2 * C1:C(3) = 3.3 * C1:C4 = 2
120   REM M & M1 = 25K & 24.5K OHMS, ADJUSTED SO CAP VALUES ARE IN UF; PL=
      # OF POLES.
130   PRINT "ARE YOU USING AN OUTPUT FILTER ? ";: GOSUB 560
140   IF X = 1 THEN  INPUT "IS THIS A 1 OR 2 POLE FILTER ? ";PL
145   HOME : PRINT "VALUES INDICATED FOR C2 AND C3 ARE FOR THE AD637 AND A
      D536A RMS CONVERTERS"
146   PRINT " FOR THE AD636,VALUES FOR THESE CAPACITORS MUST BE"
147   PRINT "2.5 TIMES THE AMOUNT SHOWN FOR THE SAME % RIPPLE AND ERROR"
150   READ SAMPLES: FOR S = 1 TO SAMPLES: READ F(S)
160 E(S) = 1 / (0.16 + (6.4 * (T ^ 2) * (F(S) ^ 2))):RD = E(S): GOSUB 550
      :E(S) = RD
170 R(S) = 50 / ((1 + ((40) * (T ^ 2) * (F(S) ^ 2))) ^ 0.5):RD = R(S): GOSUB
      550:R(S) = RD
180   ON PL + 1 GOTO 190,210,250
190   REM CAVG ONLY CALCULATIONS
200 AV(S) = R(S) + E(S): GOTO 290
210   REM 1 POLE CALCULATIONS
220 R2(S) = R(S) / (1 + (12.57 * F(S) * C(2) * M) ^ 2) ^ .5:RD = R2(S): GOSUB
      550:R2(S) = RD
230 R3(S) = R(S) / (1 + (12.57 * F(S) * C(3) * M) ^ 2) ^ .5:RD = R3(S): GOSUB
      550:R3(S) = RD
240 AV(S) = R2(S) + E(S):A2(S) = R3(S) + E(S): GOTO 290
250   REM 2 POLE SALLEN-KEY CALCULATIONS
260 R3(S) = R(S) / (M1 * C(2)) ^ 2 / ((1 / (M1 * C(2)) ^ 2 - (12.57 * F(S
      )) ^ 2) ^ 2 + (25.13 * F(S) / (M1 * C(2))) ^ 2) ^ .5
```

```
270 RD = R3(S): GOSUB 550:R3(S) = RD
280 AV(S) = R3(S) + E(S)
290  NEXT S
300 X = 2: GOTO 320: REM  PRINTOUT RESULTS
310  PR# 1: PRINT  CHR$ (29): REM CTRL SHIFT M, FOR IDS 440, 10 CHAR./''
320  HOME : PRINT "OUTPUT RIPPLE AND AVERAGING ERROR ARE": PRINT "CALCULA
     TED FOR ";
330  ON PL + 1 GOTO 340,350,360
340  PRINT C1;" UF GAVG ONLY": GOTO 370
350  PRINT "G2= ";G(C4);"UF, GAV= ";C1;"UF": GOTO 370
360  PRINT "2 POLE SALLEN-KEY FILTER": PRINT "G2 AND C3 =";G(2);" UF, CAV
     G= ";G1;" UF"
370  PRINT : PRINT "FREQUENCY DG ERROR  RIPPLE    AVG ERROR"
380  FOR S = 1 TO SAMPLES
390 B$ =  STR$ (F(S)) + " HZ":B = 10 -  LEN (B$):B2$ =  STR$ (E(S)) + "%"
     :B2 = 10 -  LEN (B2$)
400  ON PL + 1 GOTO 410,420,440
410 B3$ =  STR$ (R(S)) + "%":B4$ =  STR$ (AV(S)) + "%": GOTO 450
420  IF C4 = 2 THEN B3$ =  STR$ (R2(S)) + "%":B4$ =  STR$ (AV(S)) + "%": GOTO
     450
430  IF C4 = 3 THEN B3$ =  STR$ (R3(S)) + "%":B4$ =  STR$ (A2(S)) + "%": GOTO
     450
440 B3$ =  STR$ (R3(S)) + "%":B4$ =  STR$ (AV(S)) + "%"
450 B3 = 10 -  LEN (B3$): PRINT B$; SPC( B);B2$; SPG( B2);B3$; SPG( B3);B
     4$
460  NEXT
470  IF PL <  > 1 OR G4 <  > 2 THEN 520
480  PRINT : PRINT : PR# 0: PRINT "HIT ANY KEY TO CONTINUE": GET A$:C4 =
     C4 + 1
500  GOTO 320
520  PRINT : PR# 0: PRINT "TRY OTHER VALUES ? ";: GOSUB 560
530  IF X = 2 THEN  END
540  RESTORE : GOTO 80
550 RD =  INT ((RD * 1000) + .5) / 1000: RETURN : REM ROUND ROUTINE
560  GET E$:X = 2: IF E$ = "Y" THEN  PRINT "YES":X = 1: RETURN
570  IF E$ <  > "N" THEN X = 3: PRINT : PRINT "PLEASE REENTER";: GOTO 560

580  PRINT "NO": RETURN
590  DATA  11,1,2,4,10,20,40,60,100,200,400,1000
600  REM 1ST PIECE OF DATA CONTAINS AMOUNT OF SAMPLES TO BE READ (20 MAX)

610  REM REMAINDER OF DATA IS FREQUENCY IN HZ
```

PROGRAM #2

RMS CONVERTER COMBINED SETTLING TIME PROGRAM

```
10   REM  PROM ANALOG DEVICES SEMICONDUCTOR
20   REM  WRITTEN BY CHARLES KITCHIN AND ANDREW WHEELER MARCH 22,'83
30   REM PROGRAM TO CALCULATE 1% SETTLE TIME FOR SINEWAVE BURST
40   PRINT "********************************"
50   PRINT  SPG( 11);"AD637"
60   HOME : PRINT "COMBINED SETTLING TIME PROGRAM"
70   PRINT "********************************"
80   INPUT "ENTER CAVG (C1) VALUE IN UF : ";CAV
90   INPUT "ENTER G2 VALUE (NO G2= 0UF) : ";C2
100  INPUT "ENTER VALUE OF G3 (NO C3= 0UF) : ";C3
110 S(1) = .025 * CAV * 4.6
120 S(2) =  SQR ((S(1) ^ 2) + ((.025 * C2 * 4.6) ^ 2))
130 S(3) =  SQR ((S(1) ^ 2) + ((.025 * C2 * 4.6) ^ 2) + ((.024 * C3 * 4.6
     ) ^ 2))
140  FOR A = 1 TO 3:S(A) =  INT ((S(A) * 10000) + .5) / 10000: NEXT
150  PRINT "THE SETTLING TIMES EQUAL...": PRINT
160  PRINT S(1);" SECONDS FOR CAV ONLY"
170  IF C2 = 0 THEN 210
180  PRINT : PRINT S(2);" SECONDS FOR CAV & G2"
190  PRINT : IF G3 = 0 THEN 210
200  PRINT S(3);" SECONDS FOR GAV AND": PRINT " 2 POLE SALLEN-KEY FILTER.
     "
204  PRINT : PRINT "NOTE:"
205  PRINT "THESE VALUES ARE FOR THE AD637 AT ALL INPUT SIGNAL LEVELS"
206  PRINT "HOWEVER,FOR THE AD536A AND AD636,SETTLING TIME INGREASES AT L
     OW LEVELS.THIS INCREASE BEGINS AT INPUT LEVELS BELOW 200MV FOR THE A
     D536A AND AT LEVELS BELOW 80 MV WHEN USING THE AD636"
210  PRINT : PRINT "PERFORM ANOTHER CALCULATION ? ";: GET A$
220  IF A$ = "Y" THEN  PRINT "YES": GOTO 80
230  IF A$ <  > "N" THEN  PRINT : GOTO 210
240  PRINT "NO": END
```

ANALOG DEVICES

RMS to DC Conversion Application Guide